FUNCTION AND APPLICATION OF THE SWITCH MODE POWERSUPPLY IC

TDA 4605

Technical Manual for the integrated control circuit
for self oscillating flyback converter power supplies
with MOSFET power switching transistors

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BU2 90 = 5 AMP.
BU2 90A = 2 AMP.

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1. Introduction

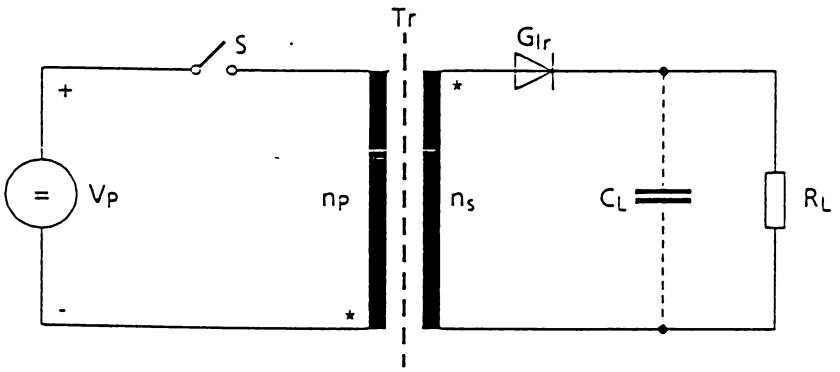
In recent years, switched-mode power supplies (SMPSs) have gained considerable importance, even in the smaller power ranges (10W to 100W). The self oscillating flyback converter has proved to be a reliable concept that requires minimum circuitry.

As prices are falling, power MOSFETS as power switches are becoming more and more attractive, not only as a result of their switching characteristics, but especially due to the low circuitry requirements for driving them. The TDA 4605 integrated control circuit allows flyback converter power supplies to be designed using MOSFET power switches with a minimum of external components.

2. Fundamentals

A flyback converter essentially consists of dc voltage source, transformer, switch, rectifier, and load (Fig. 1). The flyback converter has two operating phases. During the forward phase switch S is closed . A current flows from the voltage source via switch S and the primary winding of transformer T_r. In this process, the transformer absorbs electrical energy, and stores it magnetically. During the flyback phase, the switch interrupts the current flow . The transformer winding voltages reverse, and the transformer transfers the magnetically stored energy to load R_L via rectifier G_{lr}.

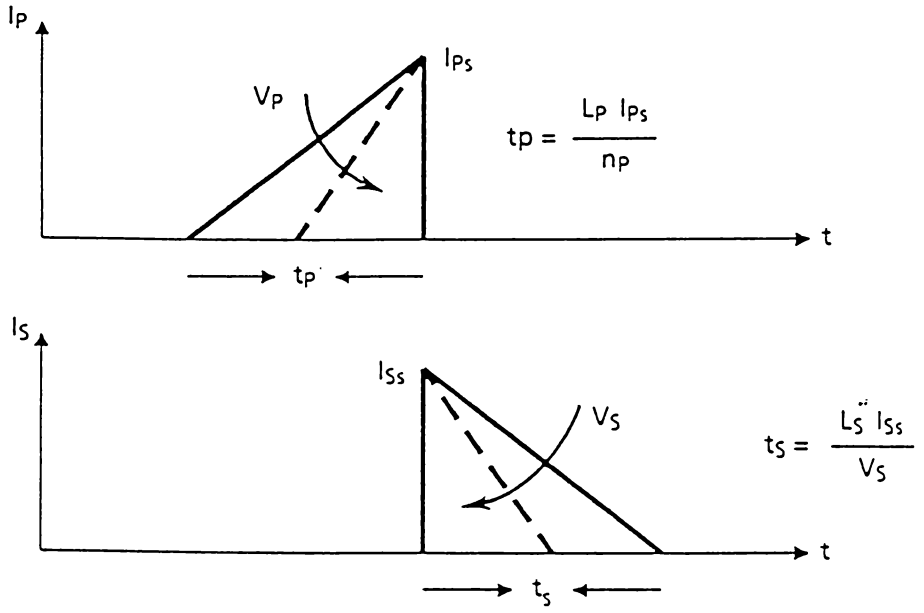
Fig. 2.1: Block diagram of a flyback converter



The transformer has n_p windings on the primary side, n_s windings on the secondary side, and a primary winding inductivity L_p. The voltage source has voltage V_p, and there is a voltage drop V_s across load and rectifier. Voltage V_p is available across the primary winding during the conductive phase. Current I_p in the primary winding rises at a rate which is determined by V_p and L_p. The switch breaks the primary circuit when the value of the current reaches I_{ps}. The current flow changes from the primary to the secondary side and starting with peak value I_{sp}, decreases at a rate which is determined by secondary nductivity L_s and voltage V_s.

Capacitor C_L, parallel to the load, smoothens the load voltage. Flyback converter SMPSs are characterized by the fact that their operation is based on a rectified and smoothed line voltage, when required. Suppose the following:

Fig. 2.2 Primary and secondary winding current characteristics



Given

$$n_P \cdot I_{Ps} = n_s \cdot I_{Ss}$$

and

$$\frac{L_p}{n_P^2} = \frac{L_s}{n_s^2}$$

the following is obtained:

$$t_s = \frac{L_P I_{Ps}}{V_s} \cdot \frac{n_s}{n_P}$$

The self oscillating flyback converter is characterized by the fact that a new forward phase starts as soon as the magnetic energy has been transferred to the load.

Time intervals t_p and t_s are used alternately.

The operating frequency is thus given by:

$$f = \frac{1}{t_P + t_s} = \frac{n_P}{L_P \, I_{Ps}} \cdot \frac{1}{(\frac{n_P}{V_P} + \frac{n_s}{V_s})}$$

The energy transferred in one operating cycle is given by:

$$W = I_{Ps}^2 \; \frac{L_P}{2}$$

The transferred power is thus given by:

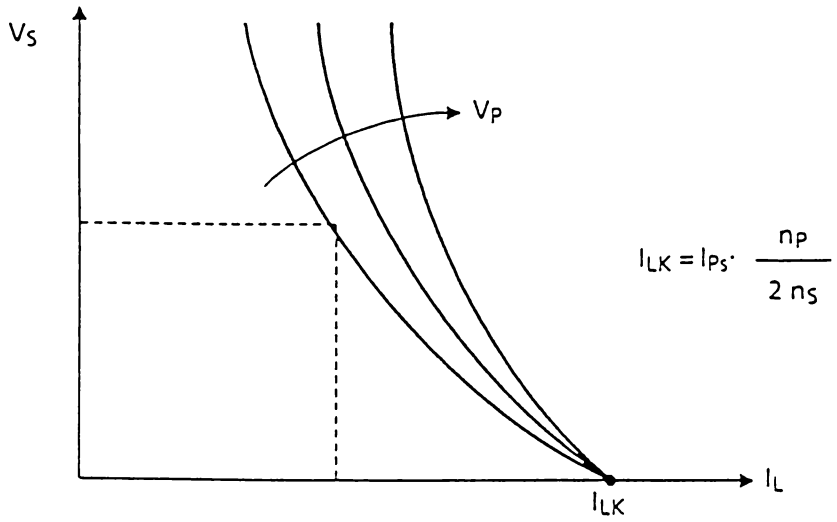
$$P = W \cdot f = I_{Ps} \cdot \frac{n_P}{2(\frac{n_P}{V_P} + \frac{n_s}{V_s})}$$

A modulation of the primary peak current I_{Ps} is thus a suitable means for regulating the power transferred by the SMPS. The magnetic flux density B in the transformer core is proportional to the primary current I_P. The maximum permissable primary peak current I_{pmax}, and hence the maximum transferred power, is thus determined by the magnetic saturation of the core.

The dc output current at the load is given by:

$$I_L = \frac{P}{V_s} = \frac{I_{Ps}}{2(\frac{V_s}{V_P} + \frac{n_s}{n_P})}$$

Fig. 2.3: Output characteristics of a self oscillating flyback converter



These output characteristics indicate that the flyback converter has a high but finite short-circuit current I_{LK}. They also show the flyback converters output voltage under no-load condition can asume rather high levels infinity and that the transferable power is largely dependent on operating voltage V_p, under ideal conditions. Switched-mode power supplies are expected to provide a rectangular output characteristic under ideal conditions: In the range of small to medium load currents, output voltage V_s should be independent of the load current. When the maximum current is attained, the output voltage should drop with an insignificant increase in the current. For IC TDA 4605 , output voltage stabilization is realized with the control amplifier and maximum current limitation with the overload amplifier. Both amplifiers modulate I_{PS} so that the desired characteristic is approximated.

The point on the output characteristic at which primary peak current I_{PS} control changes over from the control amplifier to the overload amplifier is called foldback point. TDA 4605 uses foldback point correction as a means for offsetting the dependence of the foldback point on the operating voltage V_P. The family of characteristics illustrated in Fig. 2.3 indicate that flyback converters can handle short circuits on the output side better than no-load conditions. For short-circuit conditions, the output current is always limited to a finite value, while for no-load operation, primary peak current I_{PS} must theoretically be infinitely small at the output.

The operating frequency is dependent on operating voltage V_P, output voltage V_S and manipulated variable I_{PS}:

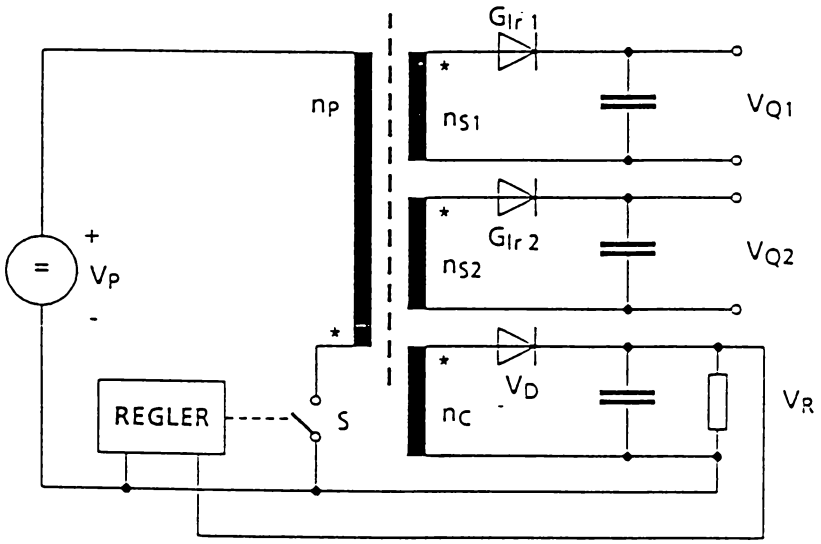
$$f = \frac{n_P}{L_P \, I_{PS}} \cdot \frac{1}{\left(\frac{n_P}{V_P} + \frac{n_s}{V_s}\right)}$$

When the output is short-circuit, V_S is as small as the forward voltage of rectifier diode G_{Ir}. Thus, the operating frequency becomes very small, too. This is why the flyback converter is essentially short-circuit resistant. Even during the start-up phase, which represents a virtual short-circuit as a result of the still uncharged smoothing capacitor C_L, the flyback converter still manifests a higher operational reliability than a flyback converter with a fixed clock frequency.

When the output voltage has reached the target value, the operating frequency is at a minimum for minimum operating voltage V_P, and maximum transferred power, i.e. maximum I_{PS}. The operating frequency increases with increasing operating voltage and decreasing power, theoretically approaching infinity if no load is applied to the output side. In practice, a capacitance combined with the transformers inductance forms a parallel resonance circuit which sets an upper limit to the operating frequency. The capacitance consists of the stray capacitances of the transformer windings, the capacitance of switch S, and the capacitance of a capacitor connected in parallel to the switch, to limit the rise time of the drain-source voltage (snubber capacitor).

In a transformer with tight magneztical coupling between the windings, the ratio of the voltages available at the windings is always the same as the ratio of their number of turns. This fact can be used to generate several regulated output voltages from a transformer and for the galvanically isolated control of the flyback converter.

Fig. 2.4: Flyback converter with several galvanically isolated output voltages.



If the regulator of Fig. 2.4 controls switch S in such a way that V_R corresponds to a specified target value, the output voltages are given by:

$$V_{Q_i} = \frac{n_{S_i}}{n_R}(V_R + V_D) - V_D$$

where V_D is the diode forward voltage (typically 0.7 V). During the blocking phase, the transformed secondary voltage adds up at switch S to produce operating voltage V_P. The voltage at the open switch is given by:

$$V_{SS} = V_P + \frac{n_P}{n_R}(V_R + V_D)$$

In self oscillating flyback converter SMPSs, the function of TDA 4605 is to drive the converter with a MOSFET power transistor so that the required output characteristics are generated and no component is damaged or destroyed.

3. DESCRIPTION OF TDA 4605

3.1 Introduction

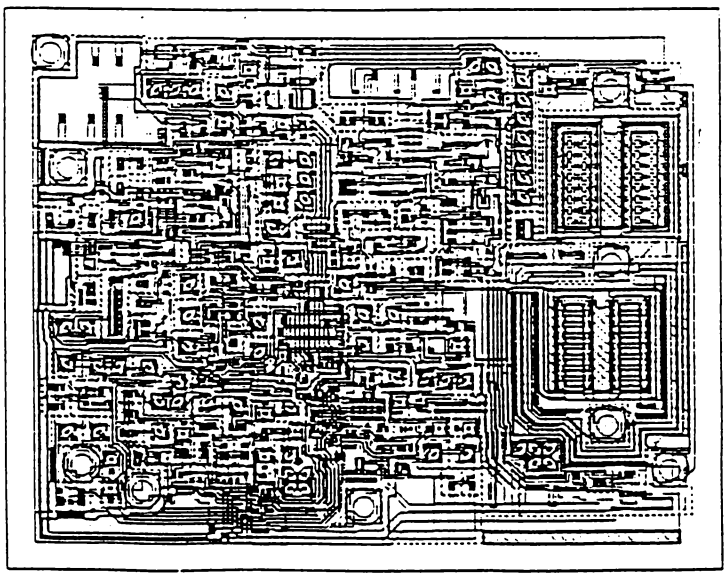
The following chapter describes the IC and its interaction with the periphery. Considerable attention is given to explaining the function of the IC to the user. Important circuitry details at the pins are therefore described and explained down to the level of transistors.

A short physical description of chip and package is followed by a functional description of the application circuit. In the subsequent sections, an explanation of the block diagram of the IC and of the individual circuits is given.

3.2 Chip and package

Fig. 3.2.1 shows the chip on a scale of 40:1.
The chip raster is 2.67mm x 2.11mm = 5.63mm^2. The chip is manufactured using 36 V standard bipolar technology. It contains approximately 300 components.

Fig. 3.2.1: Chip, scale 40:1

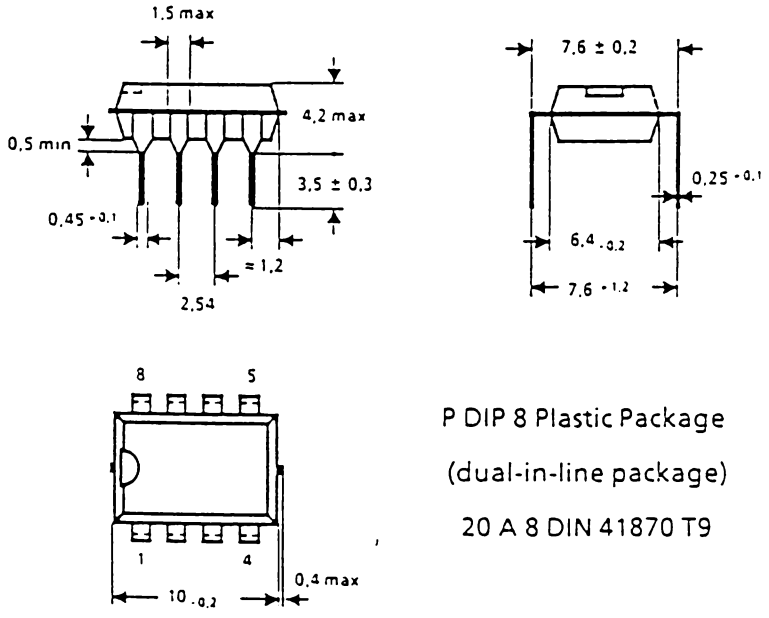


The large surface structures at the right side of the chip represent output transistors which drive the gate of the power MOSFET.

The chip is accommodated in a P-DIP 8 package, i.e., a plastic package with 8 pins. The thermal resistance R_{thJA} between system and environment is 100K/W for this package.

Thus, a power dissipation of 600 mW and more is permissible in the function range ($-20°C \leq T_A \leq +85°C$). The package dimensions are illustrated in Fig. 3.2.2.

Fig. 3.2.2: Package



P DIP 8 Plastic Package
(dual-in-line package)
20 A 8 DIN 41870 T9

The overall dissipation power is calculated by adding up quiescent dissipation power (I_q - 9 mA for U_S = 10 V) P_{VR} < 100 mW and switching losses P_{VS} which are both dependent on the connected power transistor and on the frequency. Supposing that the switching losses do not exceed 300 mW, the chip temperature $T_j = (P_{VR} + P_{PVS})R_{thJA} + T_{Amax}$ barely reaches 125°C.

3.3 Application circuit

Fig. 3.3.1 shows a possible application circuit based on the principle described in Chapter 2 . The line input voltage is rectified by D. Input capacitor C_1 smooths the voltage so that a DC voltage, i.e., the primary voltage V_P, is available at the upper terminal of the transformer's primary winding n_2. The SIPMOS transistor BUZ 90 is used as a power switch. The snubber combination D_2, R_2 and C_4 limits overshots when the power switch is turned off. Together with the stray capacitance of the transformer, capacitance C_3 determines the no-load frequency and consequently, the maximum slew rate of the drain voltage. The secondary circuit of the transformer consists of several windings, each of which has a different number of turns, polarity and loading capacity. Fusing and base load resistors are available for the rectifiers and capacitors.

The TDA 4605 IC is started using the R_1 start resistor. Capacitor C_2 is charged with half-wave currents at the voltage supply pin of the IC (pin 6). When the voltage at C_2 reaches the switch-on threshold, the switched-mode power supply starts, and supplies the KIC via winding n_1 and diode D_1.

A control voltage is generated parallel to the IC supply voltage by means of diode D_3 and charging capacitor C_6. The RC element, consisting of R_8 and C_7, prevents a peak value rectification of the high-frequency components. The divided control voltage is available at the control input pin of the IC (pin 1). The pulse width modulator of the TDA 4605 controls the duration of the forward phase, and thus, the primary peak current I_{Ppeak}, using a voltage ramp that is proportional to the drain current and has been generated with R_4 and C_5 at pin 2 of the IC. During SMPS start-up, capacitance C_8 at the soft start pin (pin 7), influences the duration of the forward phase by controlling the error voltage of the pulse width modulator. The IC detects the end of the transformer discharge phase via resistor R_9 from winding n_1. At

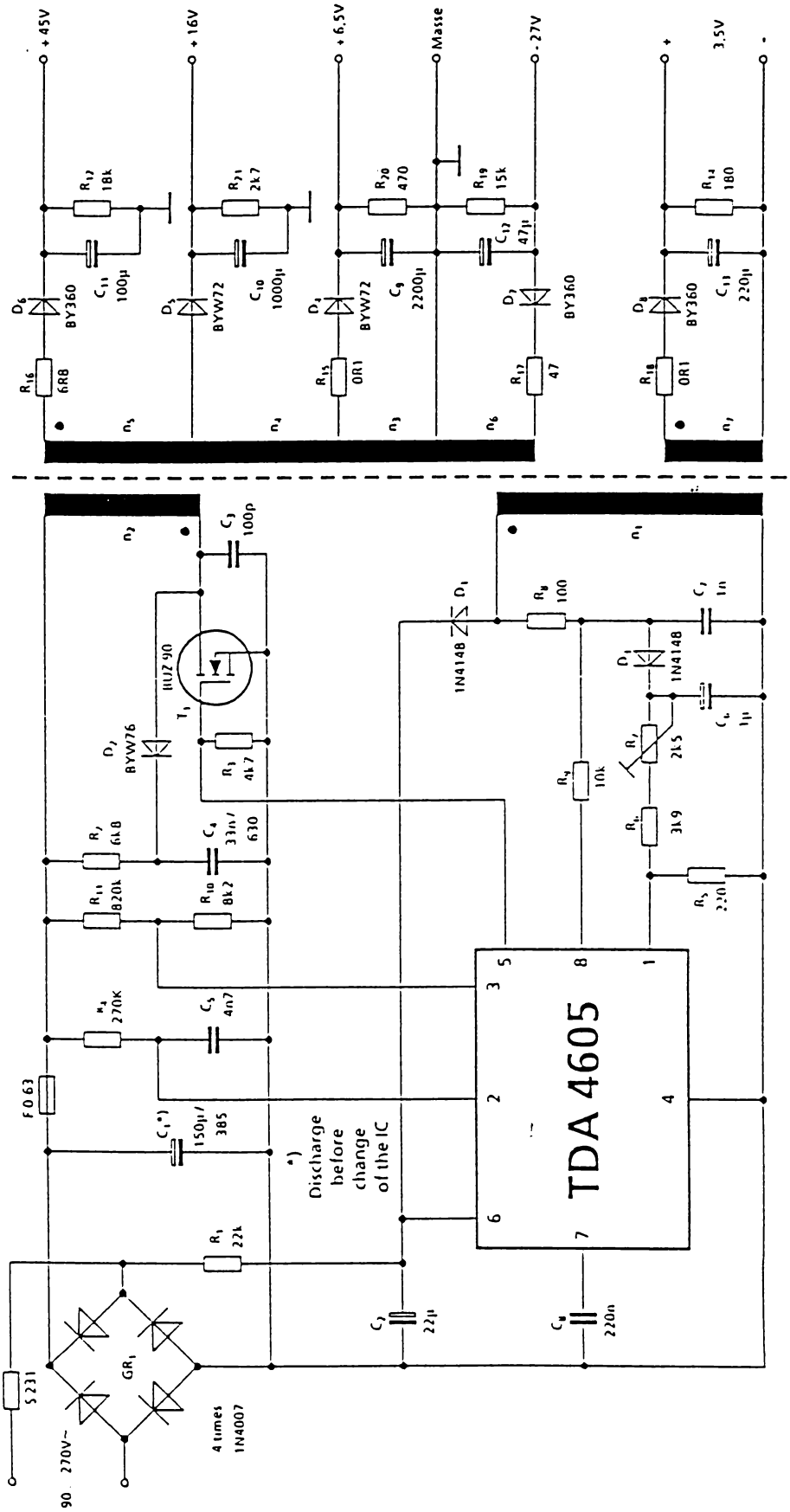
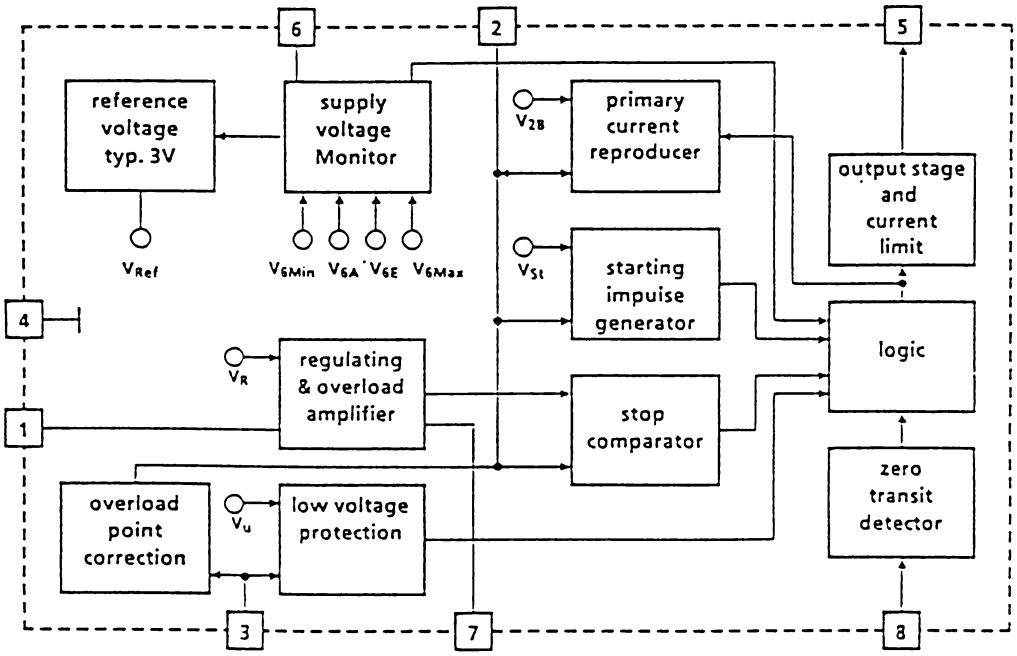


Fig. 3.3.1: Wide-range application circuit

this point, the voltage changes polarity from positive to negative. The R_{10}, R_{11} voltage divider at pin 3 of the integrated circuit is used for determining the minimum line voltage, and for foldback point correction. Chapter 4 illustrates the dimesioning of application circuit components, and in particular, the dimensioning of the transformer by means of an example. Basic design information and comments regarding the interaction with other components are given.

Block diagram



The interaction of the individual function blocks is indicated by action arrows. The subsequent listing of the pin functions is used to explain the block diagram.

Pin functions:

Pin 1

Secondary voltage information input. By comparing the control voltage from the transformer regulating winding with the internal reference voltage, the output pulse width at pin 5 is matched to the secondary side load. (normal, overload, short-circuit, no-load)

Pin 2

Information input for the primary current. The primary current rise in the primary winding is simulated as a voltage rise at pin 2 using an external RC element. The output pulse at pin 5 is terminated when a value derived from the control voltage at pin 1, is reached. The maximum power at the foldback point is adjusted using the RC element.

Pin 3

Primary voltage monitoring input. The IC is switched off at line undervoltage conditions by comparison with an internal reference. The voltage at pin 3 at the begin of the foldback point stabilisation and the voltage level for the undervoltage switch-off are in the ratio of 1.7 to 1.

Pin 4

Ground

Pin 5

Push-pull output delivers $\pm$ 1A for a rapid charge and discharge of the input capacitance of the MOS power transistor.

Pin 6

Supply voltage input. The switching thresholds V_{6A}, V_{6E}, V_{6max} and V_{6min} for operating voltage monitoring, are derived from this input. A stable internal reference voltage V_{Ref} is turned on, if $V_6 > V_{6E}$, and turned off, if $V_6 < V_{6A}$. Furthermore, the logic circuit is only enabled when $V_{6min} < V_6 < V_{6max}$.

Pin 7

Soft start input. A capacitor to ground delays the pulse duration start-up.

Pin 8

Input for oscillator feedback. After the first pulse ocurred, each zero crossing of the feedback voltage (negative-going edge) triggers an output pulse at pin 5. The trigger threshold is typically + 50 mV.
For a better understanding of the internal circuit, detailed circuit diagrams of its functional blocks are described in the following.

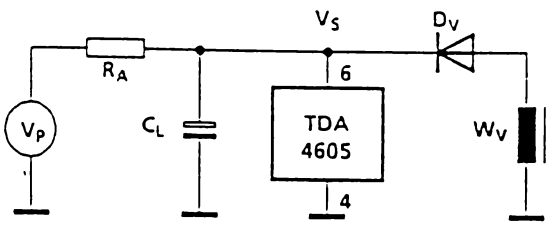
3.5 Start-up and power supply

Descriptors: Start-up circuit
Reference voltage
Current generators

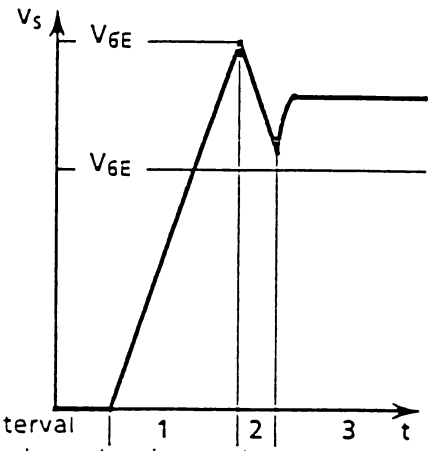
The IC is supplied via pin 6 (+ V_S). The necessary external circuitry is illustrated in Fig. 3.5.1.

Fig. 3.5.1: Supply voltage and start-up

Circuit



Voltage characteristic at C_L



The start-up sequence can be subdivided into three time intervals:

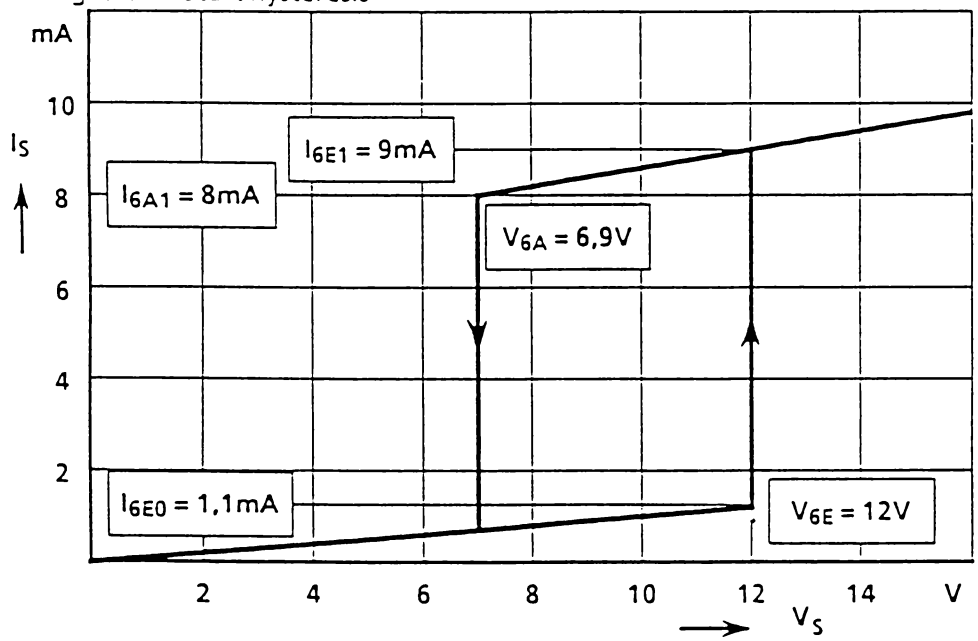
1.) Charging capacitor C_L is charged up to the switch-on voltage V_{6E} via start-up resistor R_A. In this process, the IC consumes only little power (See Fig. 3.5.2, straight line from the origin to V_{6E}). Start-up resistor R_A must be dimensioned so that sufficient power is left to charge the capacitor at minimum line voltage V_P (Caution: For half-wave charging, reduce resistance value accordingly).

2.) The IC is activated when the supply voltage reaches the switch-on voltage V_{6E}. The switched-mode power supply starts. The current consumption of

the IC exceeds the charging current; hence, a voltage drop at charging capacitor C_L.

3.) The supply winding W_V of the switched-mode power supply has flyback polarity. Diode D_V conducts if the voltage at charging capacitor C_L falls more than one diode forward voltage below the voltage available at winding W_V. Thus the capacitor CL at pin 6 is charged and the IC supply voltage increases to the selected rated value which is then regulated by the switched-mode power supply in the same way as the secondary voltages.

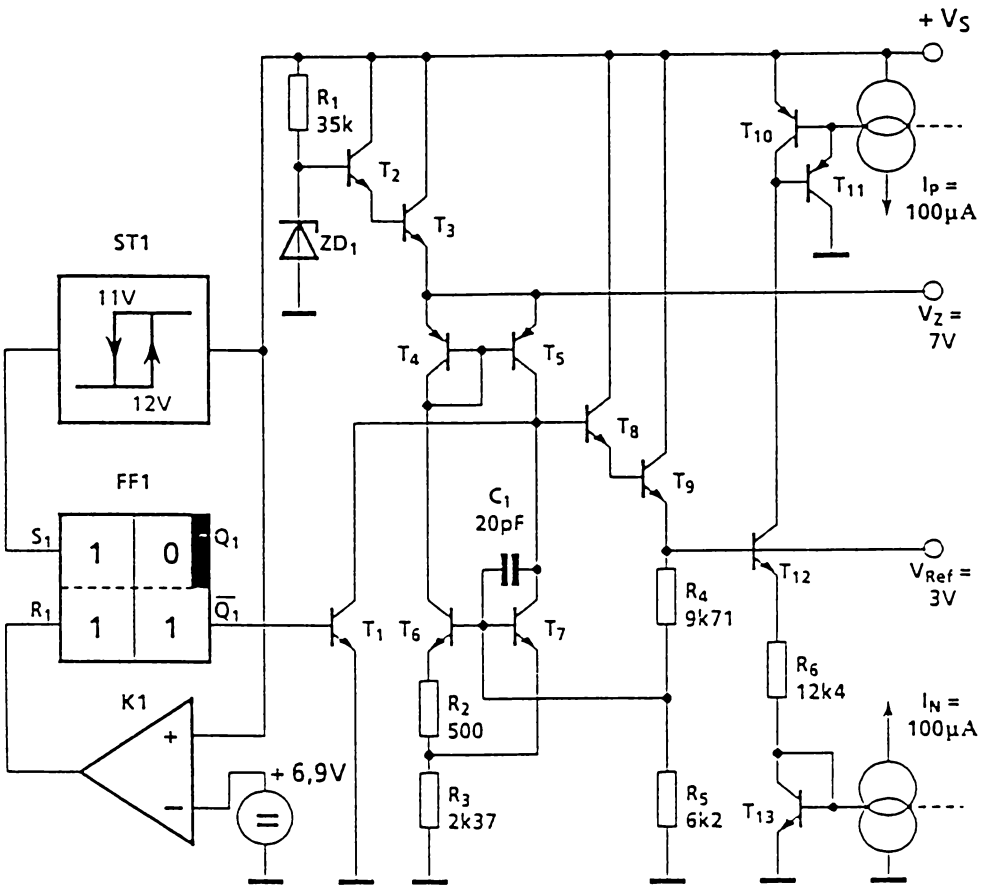
Fig. 3.5.2: Start hysteresis



The start attempt is aborted when voltage V_S reaches the switch-off threshold of the IC. This occurs especially in the case of a delayed rise in the secondary voltages, i.e. under overload or short-circuit conditions. The IC switches off causing the voltage V_F to rise again as described under 1.).

Fig. 3.5.3 shows the internal power supply of the IC. The switch-on hysteresis is generated by flip-flop FF1 (reset-dominant with the preferred state Q_1 = H), The Schmitt trigger ST1 and the comparator K1.

Fig. 3.5.3: Internal power supply circuit



The regulator circuit R_1, ZD_1 T_2 and T_3 provides the voltage V_z = 7 V. It supplies among other things a band-gap reference voltage of 1.2 V, which is amplified to V_{Ref} = 3 V. This internal temperature-independent reference voltage can be switched on and off using T_1.

The reference currents for the supply of the other stages are generated by T_{10} to T_{13}. All absolute and relative levels are derived from V_{Ref}.

3.6 Pulse generation

Descriptors : Logic circuit

Pulse width comparator (stop comparator)

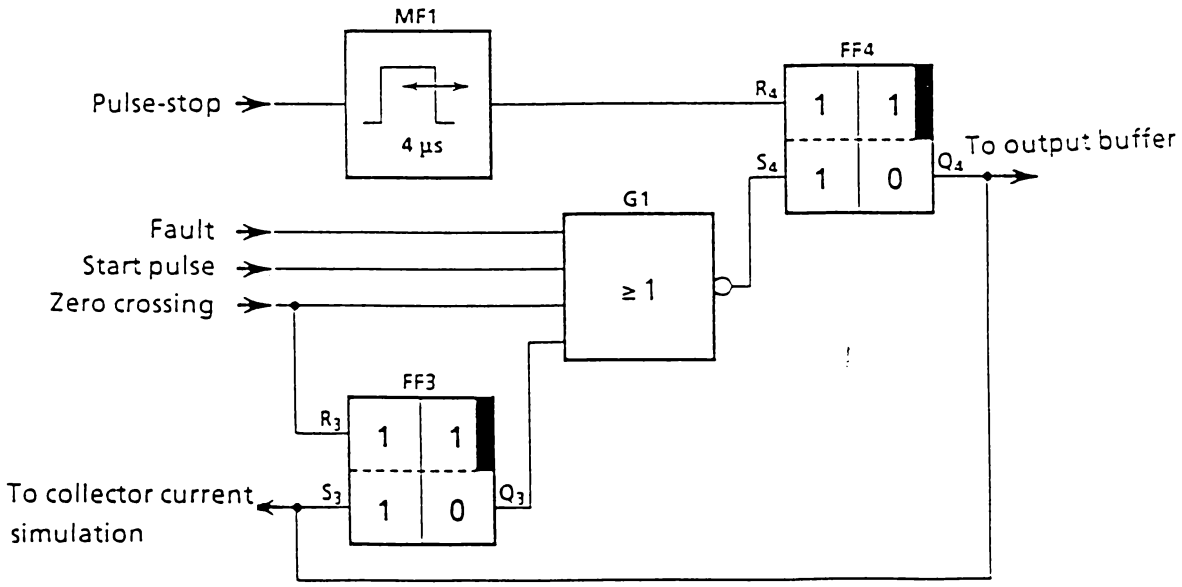
Start-pulse generation

Collector current simulation

Output stage

The logic circuit of Fig. 3.6.1 processes the start pulse, zero crossing, fault and pulse stop information and, when required, switches the output buffer circuit. The output buffer controls the power transistor gate via output pin 5. The collector current simulation is enable synchronous to the output pulse.

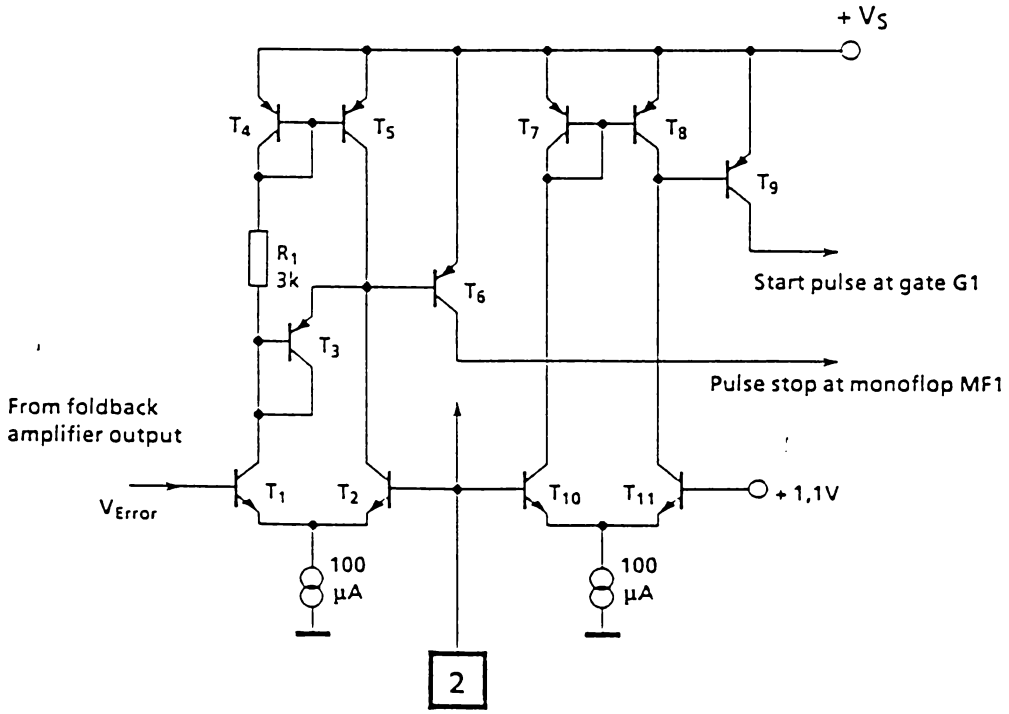
Fig. 3.6.1: Logic circuit



The pulse-stop signal is extended to typically 4 µs using the MF1 monoflop, and the reset-dominant flip-flop FF4. Start signals from the zero crossing detector, via gate G1 (in the form of a transformer ringing), are suppressed (See also transformer ringing suppression).

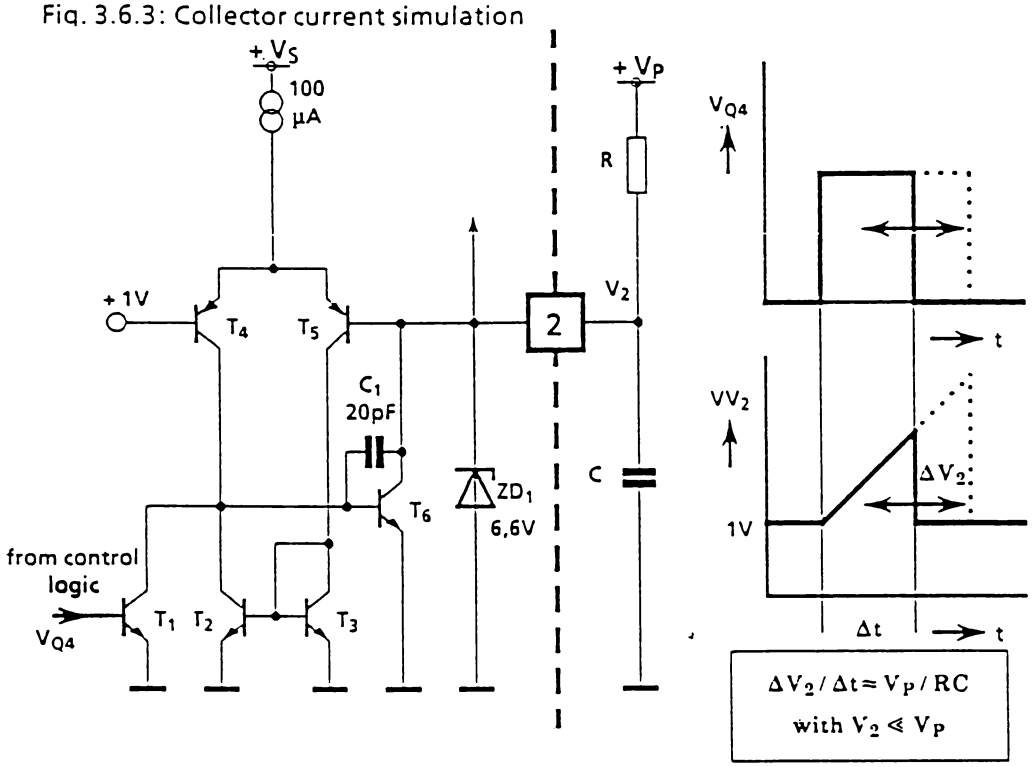
The start pulse must be generated after the IC is switched on, in order to initiate the SMPS oscillation. To this end, comparator T_7 to T_{11}, as indicated in Fig. 3.6.2, monitors the voltage at the collector current simulation pin (pin 2). Before the IC was switched on, capacitor C at pin 2 was charged from V_P to a Zener voltage of 6.6 V via resistor R (Fig. 3.6.3). Only the start pulse input at gate G1 is H after switch-on of the IC. The collector current simulation regulator in Fig. 3.6.3 discharges the external capacitor C at pin 2 down to its reference value of 1 V. The output signal at collector T_9 changes to "low" if the voltage at pin 2 falls below the comparison value of the start pulse comparator (1.1 V). This simulates a zero crossing condition to the logic circuit. The pulse stop is already dependent on the V_{error} voltage (control amplifier error signal) at the pulse width comparator (T_1 to T_6). The subsequent pulse starts are then controlled by the zero crossing detector.

Fig. 3.6.2: Pulse width comparator and start pulse comparator



T_1 in Fig. 3.6.3 clamps the base of T_6 to ground potential, if the logic circuit output U_{Q4} is H. Thus, regulator T_2 to T_6 is put out of operation, and the external RC element is charged. At the same time, the power switch is closed via the output buffer. Thus, primary voltage V_P results in primary inductance L_p. Current I_P rises according to the function $I_p = (V_p / L) \times t$. As the voltage at pin 2 rises according to the function $V_2 = (V_p / RC) \times t$ a current equivalent to the current I_p is generated. Line regulation is based on the same principle, because as the primary voltage rises, the pulse width becomes shorter.

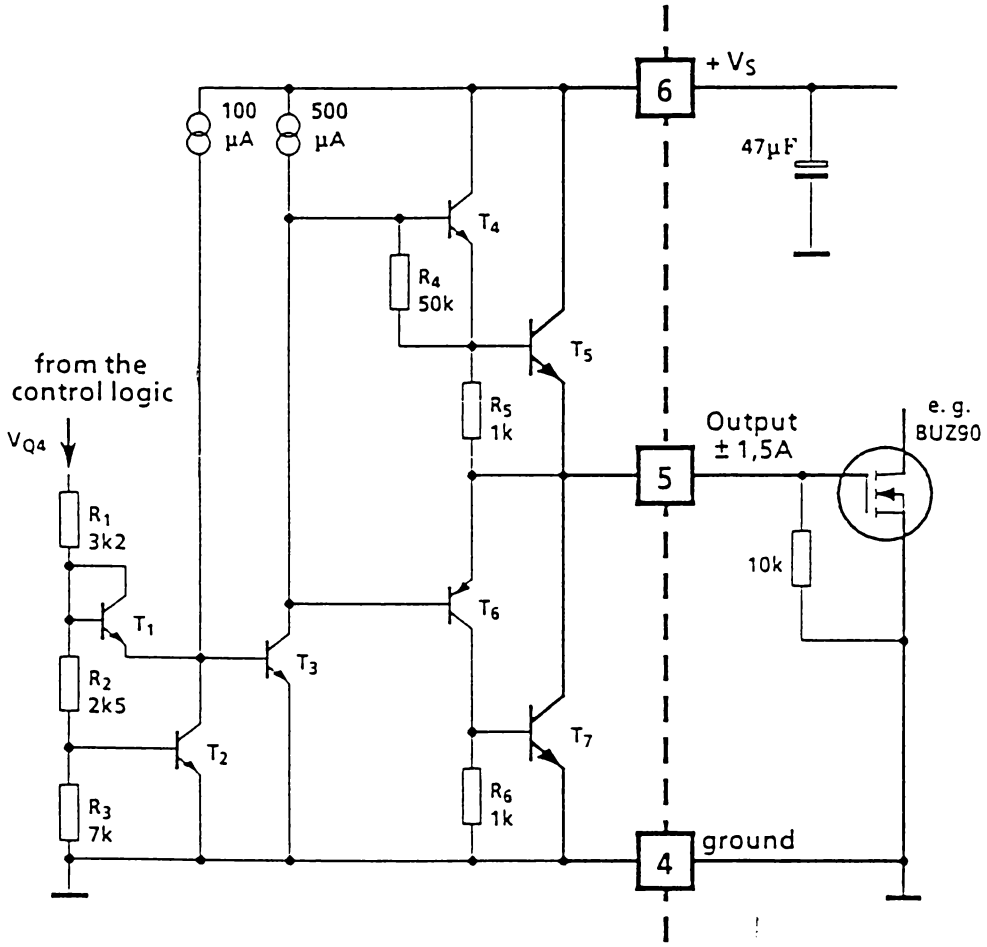
Fig. 3.6.3: Collector current simulation



The pulse width modulator consists of comparator T_1 to T_6 in Fig. 3.6.2, controller T_2 to T_6 in Fig. 3.6.3, and the external RC circuitry at pin 2. Together with the zero crossing detector, these components drive the logic circuit.

The logic circuit output signal is available at the output stage. The level converter T_1 to T_3 in Fig. 3.6.4 converts the TTL logic level to the supply voltage level.

Fig. 3.6.4: Output stage



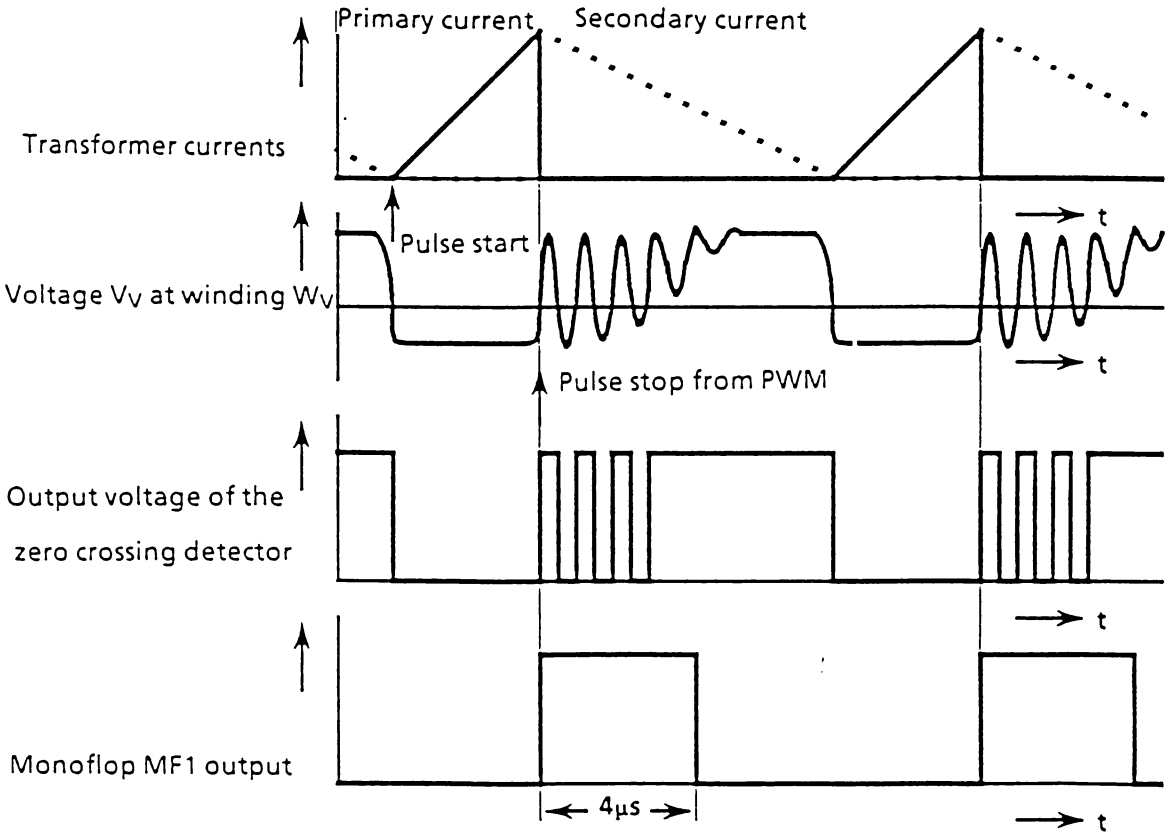
A type C push-pull output stage (T_4 to T_7), with a dead zone of approximately 2 V, is connected to its output. The output pin 5 supplies a peak current of up to ± 1.5 A for driving the input capacitance of the power transistor. The resistor, which is externally connected from pin 5 to ground, prevents static charging of the gate when the IC is switched off.

3.7 Demagnetization monitoring

Descriptors: Zero crossing detector,
Transformer ringing suppression

The zero crossing at regulating winding W_V, which is also the IC supply winding, is used for monitoring transformer demagnetization. As indicated in Fig. 3.7.1, the voltage drops to below zero, when the energy on the secondary side has been dissipated.

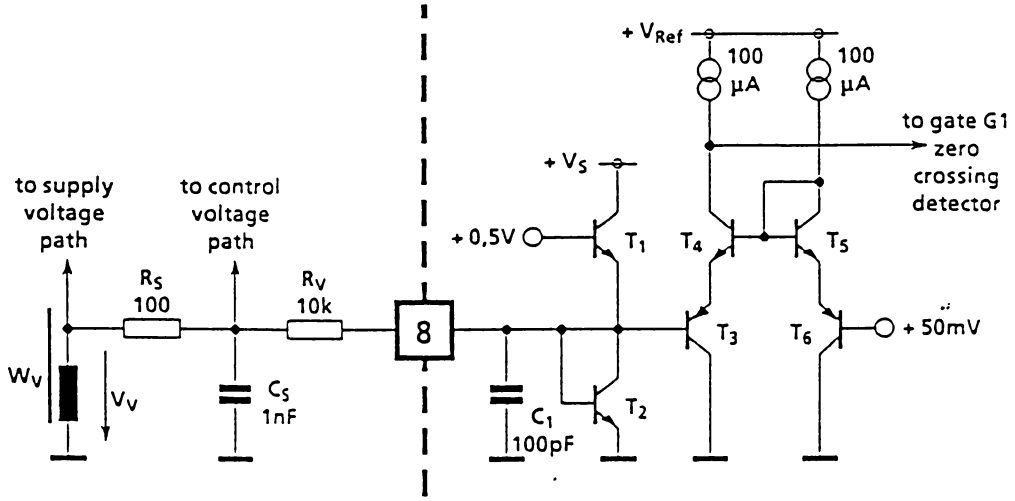
Fig. 3.7.1: Zero crossing and transformer ringing suppression



The zero crossing signal passes through a current limit resistor into the input of the zero crossing detector pin 8. The detector circuit is illustrated in Fig. 3.7.2. High-frequency overshoots are suppressed using capacitors C_S and C_1. The input range is limited with T_1 to approximately -0.2 V, and with T_2 to +0.7 V.

The differential amplifier (T_3 to T_6) then compares the signal with a reference voltage of approximately 50 mV. The amplified non-inverted logic signal is available at its output (input signal for gate G1).

Fig. 3.7.2: Zero crossing detector



The offset voltage of the differential amplifier reliably provides a low potential at the output of the zero crossing detector if "Input voltage = Zero" (starting instant of the SMPS). Thus, the start information from the start pulse comparator can be passed through gate G1 (Fig. 3.6.1) unimpeded.

When the power transistor is switched off, parasitic transformer elements generate an oscillation which may also include new zero crossings from H to L (the so-called transformer ringing). The zero crossing detector outputs this signal to the logic circuit and would start the next charging pulse. These double or even multiple pulses would overload the transformer. The transformer would go into saturation, and the power transistor would be destroyed due to overloading. These double or multiple pulse, however, cannot be generated, as they are filtered out by the transformer ringing suppression. To achieve this, the pulse stop signal is extended to typically 4 µs using monoflop MF1 in Fig. 3.6.1. As flip-flop FF4 is reset-dominant, start informations during this period are ignored. The lower signal in Fig. 3.7.1 illustrates the extented reset-dominant pulse in relation to the pulses crated by transformer ringing.

3.8 Closed-loop control

Descriptors: Control circuit,
Control and foldback amplifiers,
Soft start,
Load characteristic,
Foldback point,
Burst operation point.

The SMPS should generate voltages that are largely independent of primary voltage and loading conditions.

This is most easily attained by a right coupling between the cxontrol winding (in our case this winding is also the supply and zero crossing detector winding W_V) and the dominant secondary winding. The signal from this winding is processed so that a positive control voltage is obtained, which, as is shown in Fig. 3.8.1, is smoothed, divided accordingly and supplied to control input pin 1 of the IC. The low pass filter, consisting of a 100Ω resistor and the capacities (1n and 1µF, prevents parasitic overshoots from being peak rectified.

Fig. 3.8.1: Control circuit.

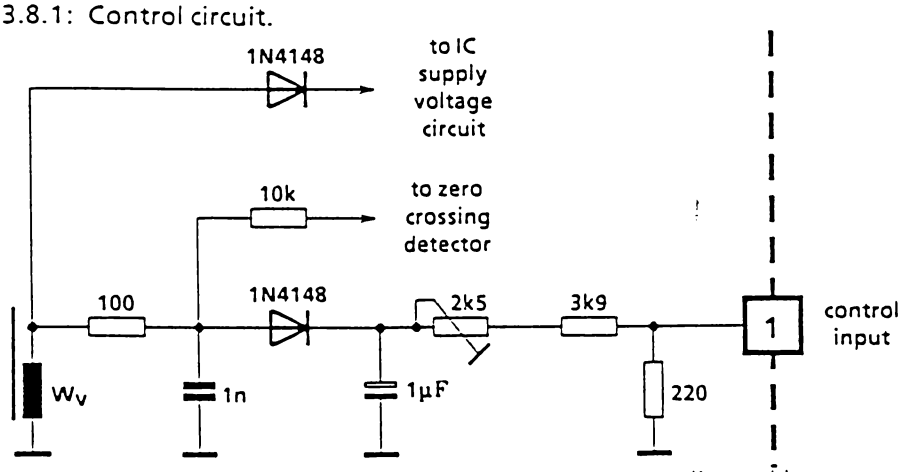


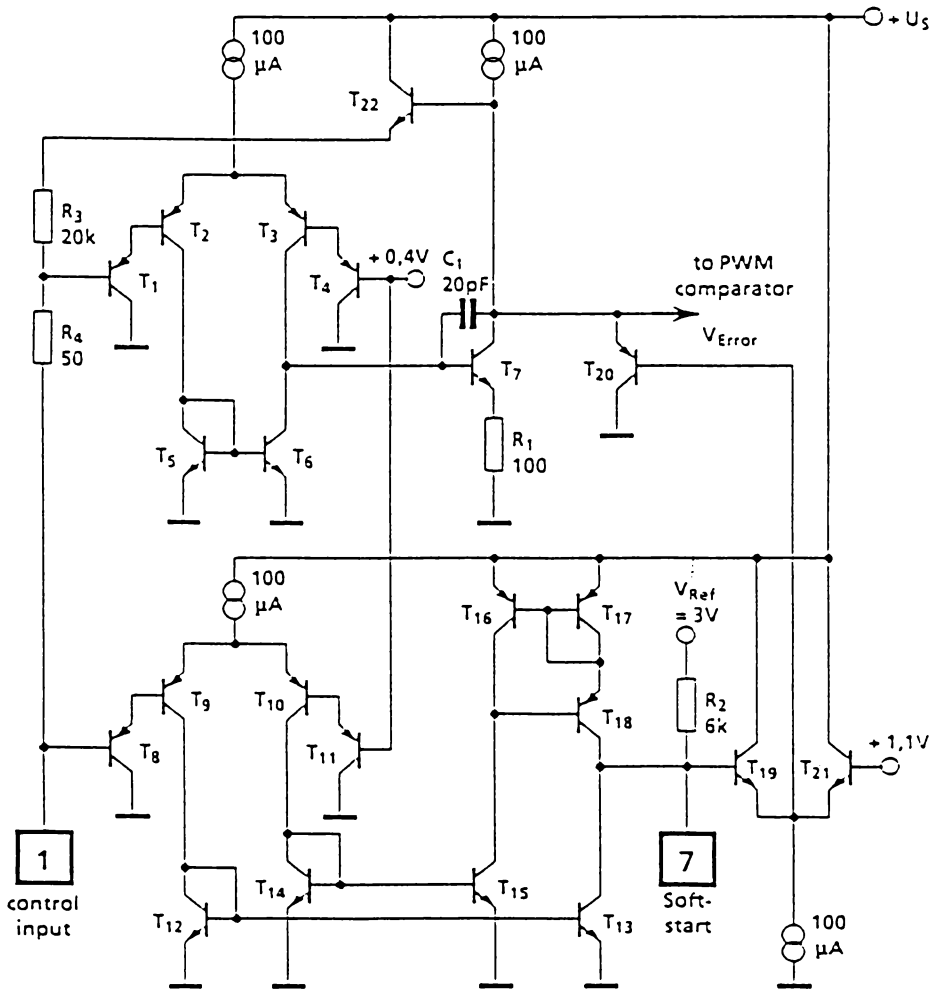
Fig. 3.8.1 is smoothed by a 1µF capacitor. This voltage is adjusted by a tresistive divider and supplied to control input pin 1 of the IC.
The control voltage, after being divided to a typical value of 400 mV, is compared with an internal reference in the IC.

Fig. 3.8.2. shows a simplified scematic of the entire control and foldback circuit. The differential amplifier (T_1 to T_6), with the connected common emitter stage (T_7) is incorporated in a negative feedback circuit together with T_{22}, R_3 and R_4 to provide an overall amplification factor of approximately 50 dB. The error signal for driving the PWM comparator (pulse width modulation) is available at collector T_7.

At switch-on, the control input voltage (pin 0) is 0 V. T_7 is blocked and does not affect the error voltage.

The foldback amplifier (T_8 to T_{18}), a differential amplifier with the connected push-pull differential current source, has an typical amplification factor of 2, and regulates the error voltage down to approximately 2 V via the buffer (T_{19}, T_{20}).

Fig. 3.8.2: Control and foldback circuit with soft start

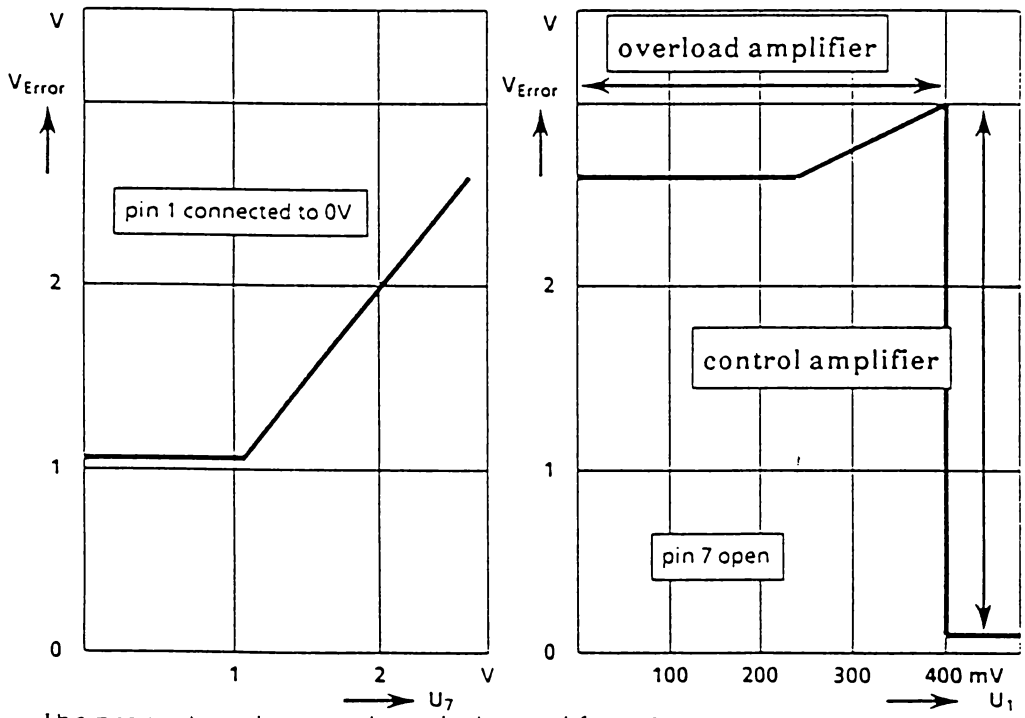


If a 100 nF capacitor is externally connected to the soft start pin (pin 7), this capacitor is charged by U_{ref} via the 6kΩ resistor R_2. Limiter T_{21} keeps the error voltage at approximately 1.1 V, and thus determines the start pulses for a soft start with 100m V_{ss} at the collector current simulation pin (pin 2).

If a secondary voltage is loaded, the control amplifier first generates the maximum pulse width (which is this pulse width, which is generated for 2 V_{ss} at pin 2). The maximum error voltage in this case is the U_{Ref} voltage at the output of the overload amplifier which is operating under balanced conditions. T_{19} and T_{20} then act to limit the error voltage.

The soft start function of pin 7 is illustrated at the left side of the transfer characteristics shown in Fig.3.8.3.

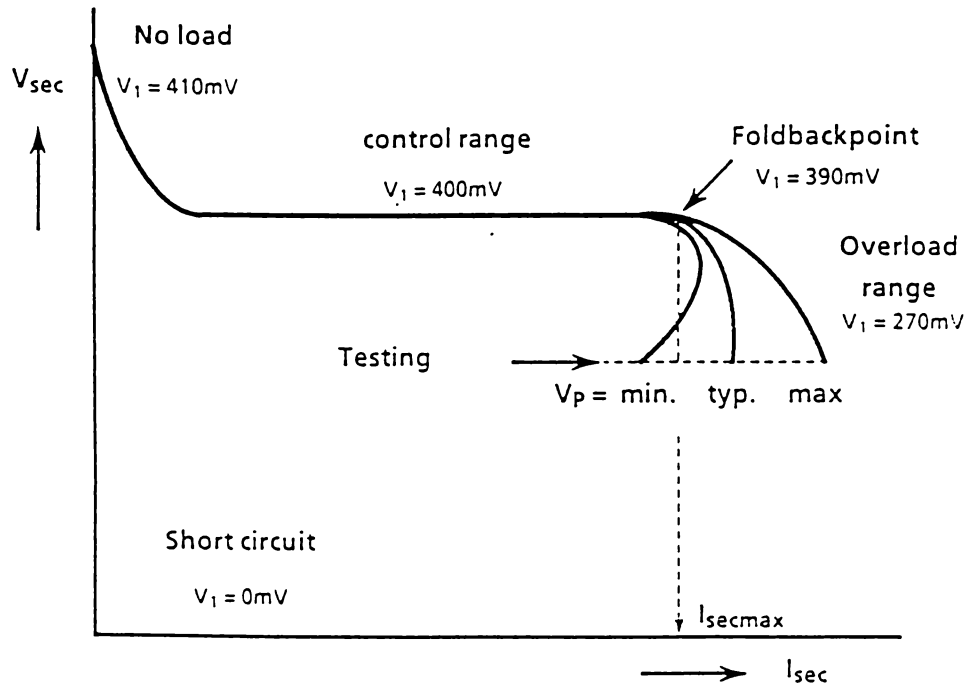
Fig. 3.8.3: Transfer characteristics



The proportional error voltage is clamped from 0 ... 1.1 V at pin 7 to 1.1 V. After this, it rises to approximately 2V in direct relation to V_7. The diagram on the right side indicates the steep gradient of the control range on the right side (Vu - 50 dB). The foldback amplifier regulates the error voltage down to

approximately 2.7 V if the control voltage decreases at pin 1, e.g. as a result of an overload condition. The error voltage remains at 2.7 V if the control voltage drops further. This control / and foldback amplifier combination generates a load characteristic, which is indicated in Fig. 3.8.4.

Fig 3.8.4: Load characteristic



The foldback point is largely independent of the primary voltage as a result of the circuit discussed in the next section.

3.9 foldback point correction

Descriptors : Constant output

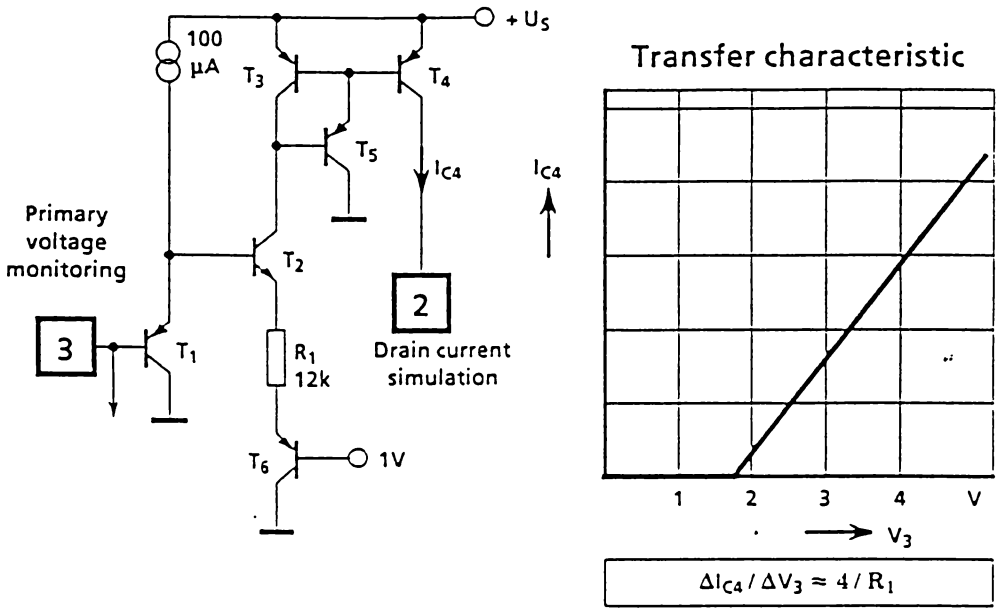
Patented design

The foldback point is the current value I_{secmax} in the secondary winding at which the pulse width modulator allows the longest primary pulse: this corresponds to the point of highest output in the load characteristic (Fig. 3.8.4). As the primary voltage U_p increases, the secondary peak current would be shifted to higher values according to the equation $I_{sec_{max}} = K_1 \times (1/(1/V_p \div K_2))$. Thus, $I_{sec_{max}}$ is a function of the primary voltage V_P and of the two constants K_1 and K_2. Foldback point correction is meant to keep the power available at the secondary winding constant by changing K1, for a given primary voltage U_p .

This is realized by influencing the collector current simulation pin. Because of the fact that the sawtooth amplitude is limited at pin 2, an external RC element can be used to adjust the maximum pulse width and this will affect the foldback point.

An additional constant current, which is dependent on the primary voltage (voltage at pin 3), is injected into pin 2, using the circuit illustrated in Fig. 3.9.1.

Fig. 3.9.1: Foldback point



The transistors T_1 and T_2 serve as a buffer, and provide, at the emitter of transistor T_2, the buffered voltage at pin 3.

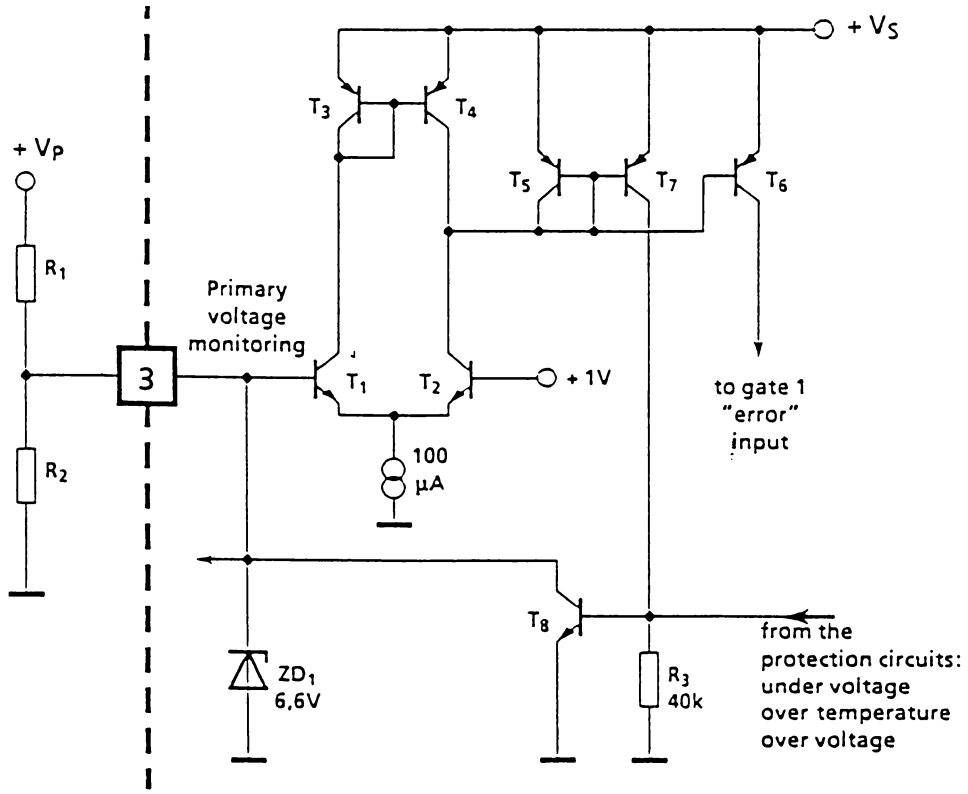
As indicated in the transfer characteristic, starting at approximately 1.7 V, at pin 3 (determined by T_6), a current flows, through T_2, which is quadrupled by T_3 to T_5 and injected into pin 2. The gradient of the transfer characteristic is determined by R_1. A patent has been applied for this method of foldback point correction.

3.10 Protective functions

Descriptors: Primary voltage monitoring,
Fault memory,
Supply voltage monitoring for over- or undervoltage conditions,
Temperature monitoring,
Response under overload conditions,
Protection against secondary overvoltage.

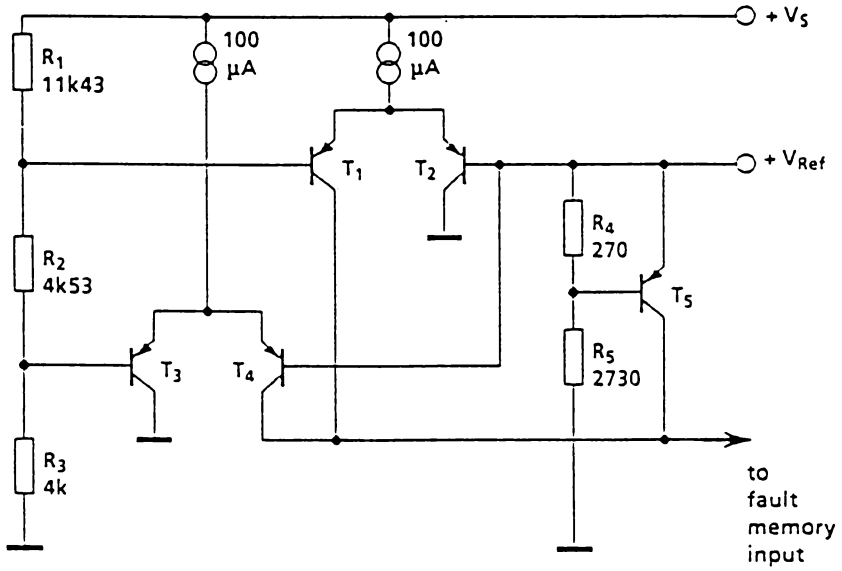
The frequency of the SMPS drops with decreasing primary voltage. It is thus necessary to switch off the SMPS, before the audibility range is reached. This is achieved by means of a comparator (T_1 to T_6 in Fig. 3.10.1) which monitors the primary voltage via the external voltage divider R_1, R_2.

Fig. 3.10.1: Primary voltage monitoring and fault memory



If the voltage at pin 3 falls below the 1 V reference voltage at the base of T_2, a fault is signaled to gate G_1 via T_5 and T_6, thus blocking the logic circuit . T_7 simultaneously generates a current and activates T_8. This positive feedback loop acts as a fault memory until the IC is switched off when supply voltage V_S < V_{6A}. The other fault informations activate the fault memory also via T_8. The circuit illustrated in Fig. 3.10.2 is used to monitor the supply voltage $+V_s$ (pin 6) for undervoltage (V_S < 7 V) or overvoltage (V_S > 15 V) conditions. Furthermore, the temperature protection circuit (R_4,R_5,T_5) switches the IC off, once a chip temperature of 150°C is reached.

Fig. 3.10.2: Protection circuits



The comparator (T_1 and T_2) signals an undervoltage condition when $U_S \leq$ 7V. This is necessary as the power transistor cannot be driven adequately below 7 V.

As the supply voltage $+U_S$ is proportional to the secondary voltage, the switched-mode power supply changes over a burst mode under overload conditions as soon as the secondary voltage has reached the burst operation point (Fig. 3.8.4). It is precisely at this point that the supply voltage of the IC falls below the undervoltage value.

If the secondary side is short-circuited behind the rectifier, the IC changes over to burst mode, as there is no supply via winding W_V. In this process, the duty cycle is reduced to between 0.01 and 0.001, as the time needed for demagnetizing the secondary side lies in the millisecond range. Consequently, the absorbed short-circuit power lies in the area of only a few watts.

The secondary voltage increases if a fault occurs in the control circuit (e.g. due to a high-resistance potentiometer). In order to limit this rise, comparator T_3, T_4 detects supply voltages exceeding 15 V and likewise activates the fault memory.
Transistor T_5, with a bias of 270 mV, becomes active when the chip temperature exceeds 150°C. If the fault memory is activated, the supply voltage collapses as there is no supply from winding W_V. As a result of this, the IC switches off and then rerstarts. Therefore all fault signals have a hysteresis.

4. TDA 4605 application

The functioning of the TDA 4605 in the application circuit has already been described in Chapter 3. The following chapter deals with the general design of the application circuit, including transformer design.

The following are given:

- Maximum total power of the switched-mode power supply P_{Tot}
- Line voltage range V_{Imin} to V_{Imax} (r.m.s. values)
- Line frequency F_I
- Rated output voltages V_{Qo}
- Maximum output currents I_{Qo}

Fig. 4.1 shows the integrated circuit TDA 4605 as part of an application circuit. The information given below is used for dimensioning the components listed in the application circuit.

Start-up resistor R_1 $\quad \frac{V mains\ max}{15 mA} < R_1 < \frac{V mains\ min}{3{,}6 mA} - 4k\Omega$

Power dissipation

$$P_{max} = \frac{V_{mains\ max}{}^2}{2 R_1}$$

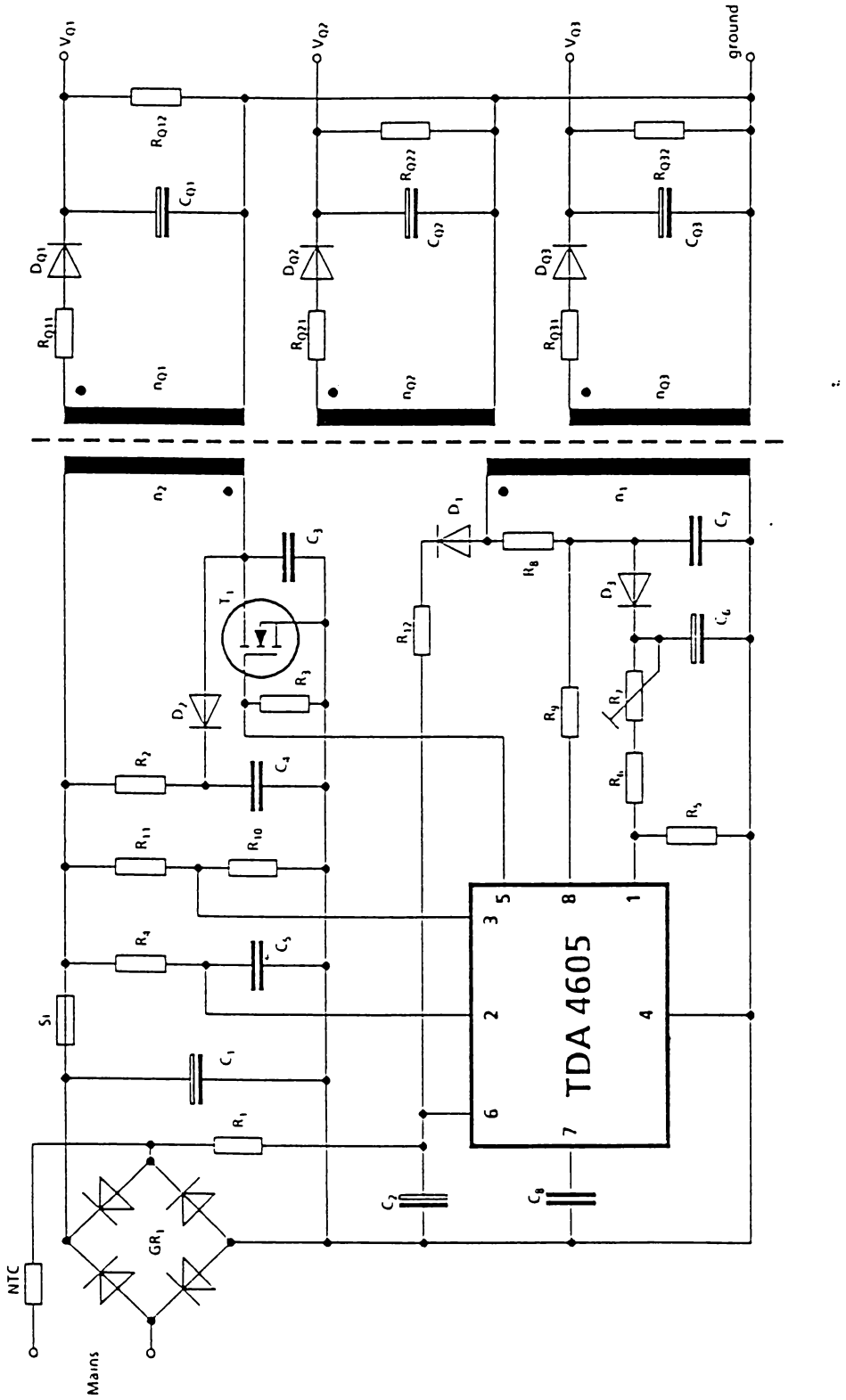
Line input capacitor C_1

$$C1 \geq \frac{2 P_{tot}}{V mains\ min^2 \cdot f_N}$$

Rated voltage

$$V_{max} = 1{,}41 \cdot V_{mains\ max}$$

Fig. 4.1 Application circuit for general design



The supply voltage range of the flyback converter is used for further dimensioning considerations.

$$V_{pmax} = 1,41\ V_{main\ max}$$

$$V_{pmin} = 1,2 V_{main\ min}$$

Voltage divider for undervoltage switch-off (R_{10}/R_{11})

$$R_{11} \geq \frac{V_{pmax}}{0,75 mA}$$

$$R_{10} = R_{11} \cdot \frac{1,1 V}{V_{pmin}} \quad (+10/-0\ \%)$$

Power MOSFET

Actual blocking voltage

$$V_{Dpeak} = V_{pmax} + V_x + V_ü$$

V_x = Voltage at primary winding during flyback phase

V_o = Amplitude of overshoots

When using avalanche-resistant MOSFETs, virtually no reserve in the U_{DSS} is required ($V_{DSS} > V_{DPeak}$); for non-avalanche-resistant MOSFETs, a voltage reserve of at least 20% mus: be allowed for ($V_{DSS} > 1.2\ V_{DPeak}$).
Any value can be choosen for V_X and V_o, but however this will affect the dimensioning of the transistor.

LINE VOLTAGE RANGE	V_{DSS} AVALANCHE -RESISTANT	V_x	V_o
180 ... 270V	600V	125V	80V
90 ... 270V	600V	125V	80V
90 ... 135V	400V	100V	80V

The conducting-state power dissipation of the MOSFET is given by

$$P_{\Omega} = R_{DSon} \cdot \frac{4}{3} \left(\frac{P_{tot}}{V_{pmin}}\right)^2 \left(1 + \frac{V_{pmin}}{V_x}\right)$$

For R_{DSon} the value at the highest chip temperature should be used . The conducting-state power and the switch turn-on power (See below) must be dissipated by means of a suitably sized heat sink.

Fuse SI

Rated current

$$I_{rated} = \frac{2}{\sqrt{3}} \frac{P_{Ges}}{V_{pmin}} \sqrt{\left(1 + \frac{V_{pmin}}{V_x}\right)}$$

Rectifier bridge G_R:

Rated voltage $V_{mains} \geq V_{mains\ max}$

Rated current for capacitive load $I_{rated} \geq \frac{P_{tot}}{V_{mains\ min}}$

NTC thermistor

Current capability $I_{max} = 2 \cdot \frac{P_{tot}}{V_{pmin}}$

Transformer

Refer to the Chapter "Cores for Power Transmission" in the Ferrite Data Handbook when selecting the transformer core. Cores with a small cross-section (EC cores) induce a smaller voltage per winding so that the ratio of the output voltages to one another can be more easily adjusted. The magnetic coupling between primary winding and secondary winding is of fundametal importance to flyback converters. The windings should therefore be interleaved. If, for production reasons, separated coil bodies for the primary and secondary winding is used, which naturally leads to a far worse coupling, the coupling should be improved by choosing a larger core.

The following are given

A = Minimum cross section of the core

B_s = Maximum magnetic flux density (retain safety margin to saturation point)

As was already discussed in Chapter 2, the operating frequency of the self oscillating flyback converter is at its lowest at minimum line voltage and maximum load. The flux density amplitude also reaches its maximum at this point. When the load of the power supply uniti is reduced, the flux density level decreases, and the frequency increases in inverse proportion. The core power dissipation increases more with the flux density level than with the frequency, and is thus at its highest at maximum load.A given ferrite core is able to transfer the highest power at maximum flux density and the highest operation frequency allowed to prevent the core from overheating. This frequency is termed f_{min} in all further calculations. The TDA 4605 IC brings optimal performance in the frequency range 20 kHz $\leq f_{min} \leq$ 50 kHz.

Hence, the number of turns is given by

$$n_{Qi} = \frac{V_{Qi} + 0{,}8V}{V_{ns}}$$

$$n_2 = \frac{V_z}{V_{ns}}$$

$$\frac{8{,}5V}{V_{ns}} \leq n_1 \leq \frac{13V}{V_{ns}}$$

The windings should be arranged so that the primary winding n_2 is coupled as tight as possible to this secondary winding having the largest power load (interleaved arrangement, if possible), and that the regulating winding n_1 is most tight coupled to this secondary winding whose voltage has the closest regulation requirements.

The transformer core must have an air gap which allows the A_L value to be ajdusted as follows:

$$A_L = \frac{1}{2} A^2 B_s^2 \cdot \frac{f_{min}}{P_{tot}}$$

If only standard values for air gap or A_L value are available, the next larger air gap (i.e. the next smaller A_L value) should be used.

Turn-to-turn voltage during the blocking phase.

$$V_{ns} = 1{,}2 \cdot f_{min} \cdot A \cdot B_s \left(\frac{V_z}{V_{pmin}} + 1\right)$$

The voltages required at the windings must exceed the output voltages by the forward voltage drop of the rectifier.

$$V_{Si} = V_{Qi} + 0{,}8V$$

The secondary voltage V_{Si} can only be set in steps of V_{ns}, as only complete windings can be wound onto the transformer. Turn-to-turn voltageV_{ns} must therefore be adjusted so that it is a common divisor of the Vsi secondary voltages. The turn-to-turn voltage can be reduced by reducing either f_{min} or B_S, whereby the transferrable power is likewise reduced. The turn-to-turn voltage can be slightly increased by increasing f_{min}. The higher core loss resulting from such an increase can be partially offset by lower copper losses.

Foldback point adjustment

The maximum voltage pulse at the primary winding, which should not cause magnetic saturation, is adjusted using the $R_4.C_5$ time constants.

$$R_4 \cdot C_5 = \frac{A \cdot B_s \cdot n_2}{2V}$$

The value of resistor R_4 should be selected as follows to optimize the foldback point correction.

$$R_4 = \frac{1}{\frac{900\mu A}{V_x} - \frac{R_{10}}{R_{11}} \cdot \frac{1}{3k\Omega}}$$

Snubber

The snubber circuit consists of C_3, D_2, C_4 and R_2. The selection of the value for capacitor C_4 will cause no major problems, can however affect dynamic control response. Typical values are in the range of 22 nF to 100nF. The dielectric strength must be at least $V_{Pmax} + V_x + V_o$.

Diode D_2 must have the same voltage rating; an additional margin of 25% is recommended. Furthermore, D_2 must have a very short forward recovery time.

The amplitude V_o of overshoots can be adjusted with R_2.

$$R_2 = V_u \cdot \frac{V_x + V_u}{P_{tot}} \cdot \frac{L_p}{L_{St}}$$

L_P is the inductance of the primary winding for open secondary windings.

L_{St} is the stray inductance of the primary winding for short-circuited secundary windings.

R_2 must be rated for

$$P_2 = \frac{V_x + V_u}{V_u} \cdot P_{tot} \cdot \frac{L_{St}}{L_p}$$

If the power dissipation of R_2 reduces the overall efficiency of the SMPS to strong, the transformer coupling must be enhanced by improving the winding technique or by choosing a core with a bigger cross-section.

Capacitor C_3 limits the slew rate of the drain source voltage of T_1. The higher the capacitance value, the easier is interference suppression, but the greater is the turn-on power loss of T_1 and the worse the closed loop staqbility at small loads. Typical values lie in the range 100 pF...500 pF. C_3 should be able to periodically cope with 10 kV/µs gradients. The turn-on power dissipation of T_1 is at a maximum for maximum line voltage and reduced power output, and is then given by

$$P_{in} = C_3 \cdot 150kHz \cdot \frac{(V_{pmax} - V_z)^2}{2}$$

Output rectifier D_{Qi}

rated voltage $$V_R \geq 1{,}5 \cdot V_{Qi} \cdot \left(\frac{V_{pmax}}{V_z} + 1\right)$$

Reverse recovery time $$t_{rr} \approx 300ns$$

R.m.s current rating $$I_{eff} \geq 1{,}2\ I_{Qi} \sqrt{\left(1 + \frac{V_z}{V_{pmin}}\right)}$$

Output capacitors C_{Qi}

Dielectric strength $$V_{max} \geq 1{,}6 \cdot V_{Qi}$$

R.m.s. current rating $$I_{eff10kHz} \geq I_{Qi} \sqrt{\left(\frac{1}{3} + \frac{4}{3} \cdot \frac{V_z}{V_{pmin\,min}}\right)}$$

Fusing resistors R_{Qi1}

Rated current rating $$I_n = 1{,}2\ I_{Qi} \sqrt{\left(1 + \frac{V_z}{V_{pmin}}\right)}$$

The resistor value is dependent on the coupling ratio. Typical values lie in the order of magnitude

$$R_{Qi1} \approx 0{,}01 \frac{V_{Qi}}{I_{Qi}}$$

For outputs whose power $I_{Qi} \cdot U_{Qi}$ is a major part of P_{Ges}. (overall power) there is no need for a resistor or a fuse ($R_{Qi1} = 0$).

Bleeder resistors R_{Qi2}

The bleeder resistors prevent the output voltage from rising when the load is disconnected. Here too, the resistor value is dependent on the coupling ratio. Typical values are given by

$$R_{Qi2} = 100 \cdot \frac{V_{Qi}}{I_{Qi}}$$

IC supply unit D_1, R_{12}, C_2

$$C_2 \geq 4\mu F/ms \cdot \frac{1}{P_{tot}} \Sigma V_{Qi}^{\,2} C_{Qi}$$

C_2 is given by the ratio of the energy stored in the output capacitors to the total output power of the power supply unit. Dielectric strength: 25 V.

R12: Typical value 10 Ω; may be omitted, if the tranformer coupling is tight enough ($R_{12} = 0$).

D_1: voltage rating

$$V_R \geq 20V + 1{,}5 \cdot V_{pmax} \cdot \frac{n_1}{n_2}$$

Current rating:

$$I_{AV} \geq 50mA$$

Soft start

The soft start response characteristic is determined by the value of capacitor C_8. The noise generated during the start-up phase is thus significantly reduced. Typical value for C_8: 220 nF. If the value for C_8 is much higher, C_2 must also be increased by the value ΔC_2.

$$\Delta C_2 = 20 \cdot C_8$$

Control circuit

Typical values:

$R_8 = 100\Omega$

$R_5 = 220\Omega$

$R_7 = 2{,}5k\Omega$

$$R_6 = \frac{V_{ns} \cdot n_1}{1{,}8mA} - 2k\Omega$$

$R_9 = 8{,}2k\Omega \ldots 10k\Omega$

D_3: 1N4148

With the above values, R5 sets the control amplifier gain an output voltage change of approximately 7% covers the whole control range. If R_8, R_5, R_7 and R_6 are halved, an output voltage change of approximately 4% covers the control range. C_6 determines the regulation time constant.

Typical value: $R_8 \cdot C_6 \approx 100\mu s$

C_7 must be such that T_1 is turned on at the first drain voltage minimum, after the transformer has outputted its energy to the load.

Typical value: $R_8 \cdot C_7 \approx 0{,}5\mu s$

5. Conclusions

The above dimensioning information provides instructions for the design of the standard application circuit. In many cases however, it is recommended that the user himself gathers experience, based on Chapters 2 and 3, in the construction of self oscillating flyback converter SMPSs, in order to be able to make optimal use of the TDA 4605 IC.

Application Eample:

200 Watt Power Supply, for Digital TV Sets

From the wide range of applications of the TDA 4605 Switch Mode Powersupply IC we selected a 200 Watt Powersupply unit for a digital TV set. The function of this powersupply shall be demonstrated to the user by means of the circuit diagram and some representativ oscillograms.

The powersupply was developed for a TV chassis with digital signal processing. Therefore it is a modern concept and can deliver a peak output power of approx. 200 W. In the technical manual the basic function of the integrated circuit and the operation of a SMPS using the TDA 4605 was explained in detail. But this application has some differences compared to the application circuit given in the technical manual:

1) The control and the IC supply voltage are derived from different windings of the power transformer. Therefore it is possible to optimize the perfomance regarding crosstalk of sound into the picture (voltages V3 and V1) and the response of the control circuits independend from the supply voltage of the integrated circuit.

2) The zenerdiode D_{103} improves the control response of the circuit.

3) The network in between the IC and the gate of the power transistor is used to optimize the powertransistor's radiated noise.

4) The RC circuit R_{115}/C_{109} allows to operate the power supply in Stand-by with only 11 Watts primary power consumption and 4 Watts of power transferred to the load.

In the following the most important waveforms measured by oscilloscope are given for the power supply according to page 47.

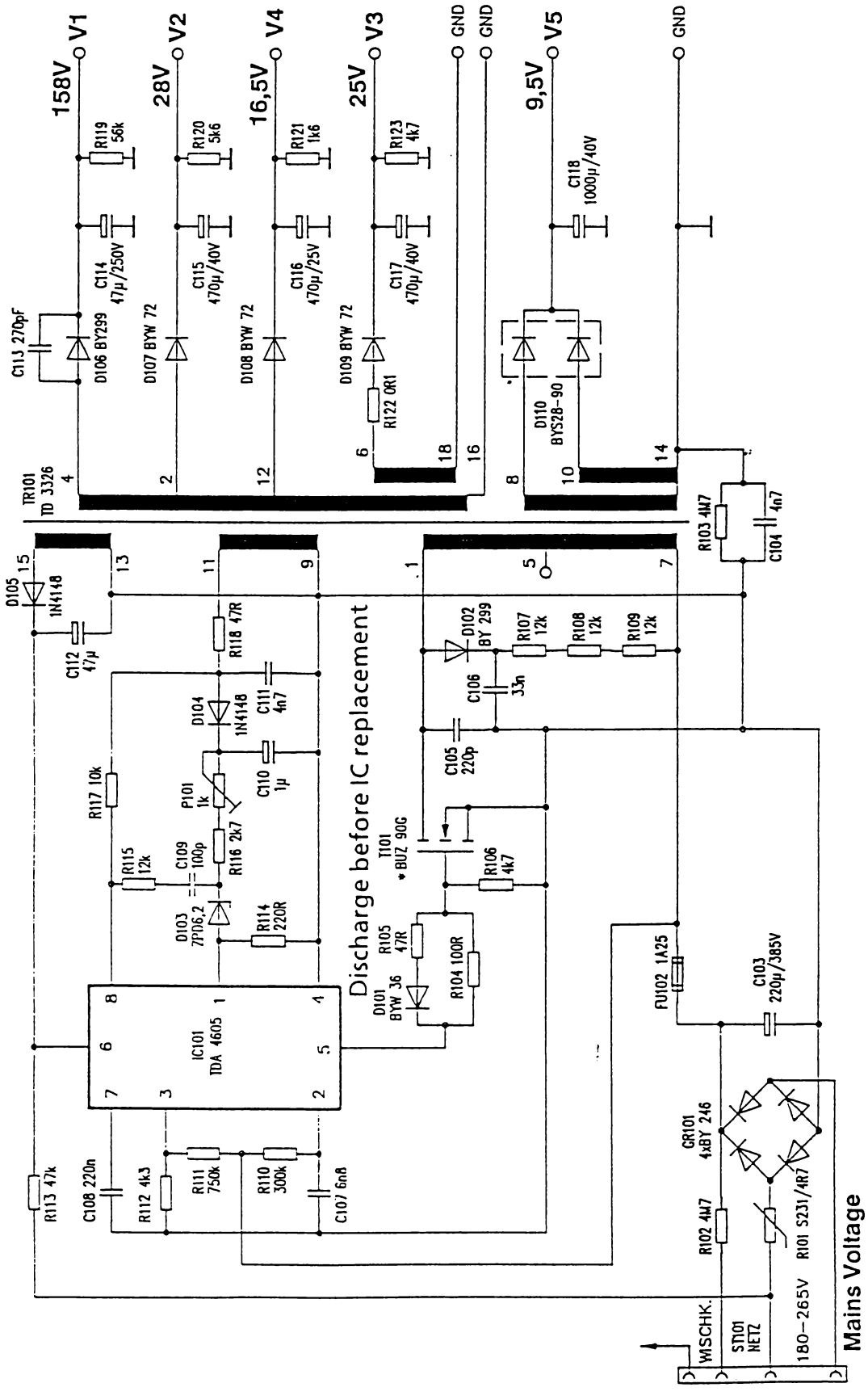
The following load conditions are used:

1) Nominal condition:

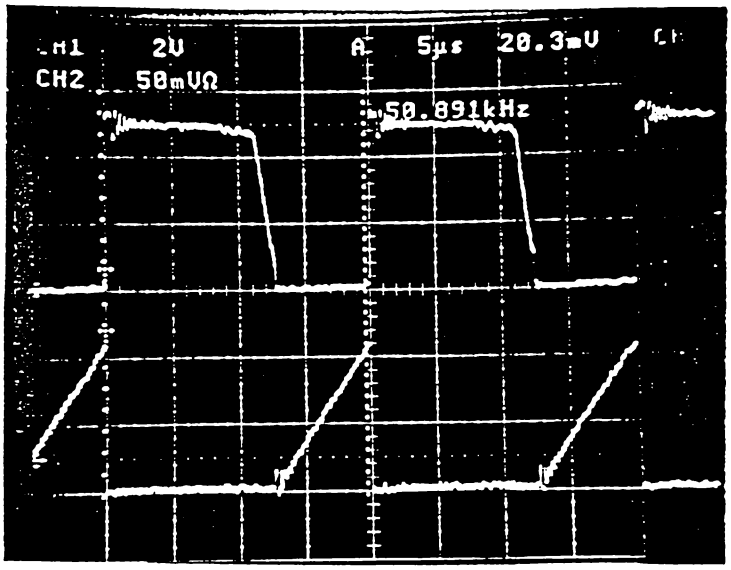
Output voltage	Load current	Outputpower
V1 = 157,0V	510mA	80,0Watt
V1 = 28,0V	190mA	5,3Watt
V1 = 25,0V	50mA	1,3Watt
V1 = 16,5V	1200mA	19,8Watt
V1 = 9,5V	1900MA	18,1Watt

Stand-by operation

Primary power consumption:	11W
Transferred power:	4W



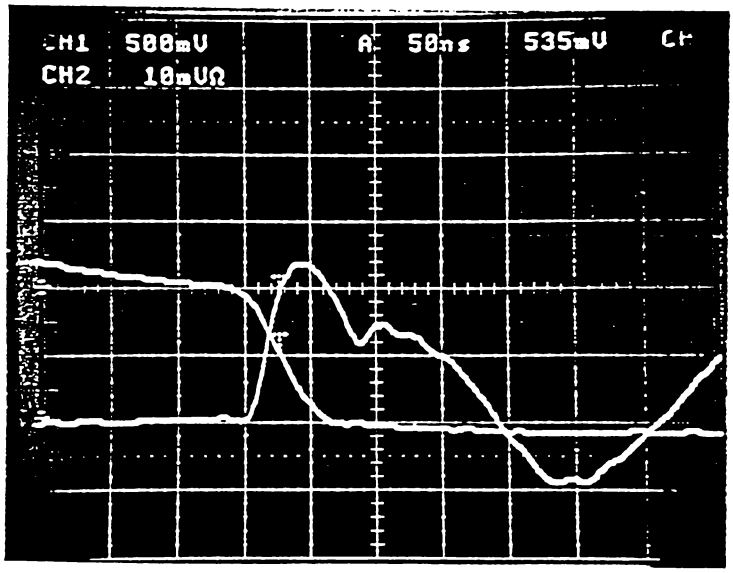
Circuit diagram: 200 Watt Power supply for digital TV



Drain voltage and Drain current

Channel 1: V_{DS}; 200 V/Div.

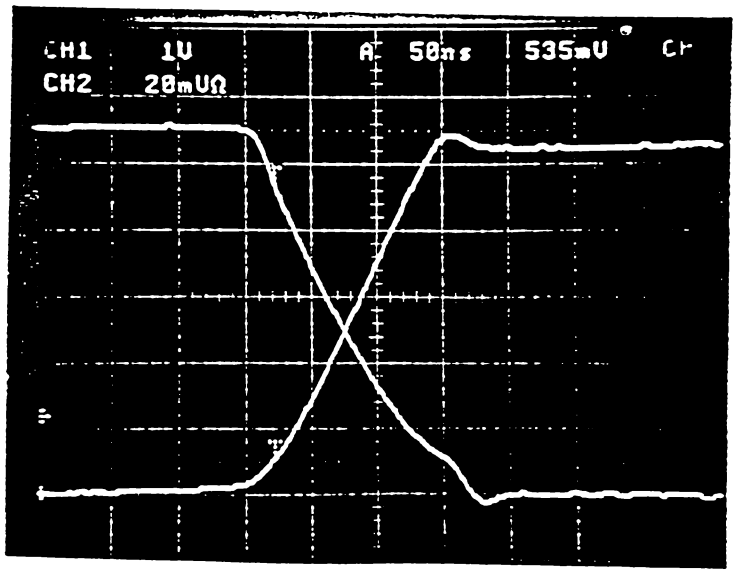
Channel 2: I_{DS}; 1 A/Div.



Turn-on Phase of the Powertransistor

Channel 1: V_{DS}; 50 V/Div.

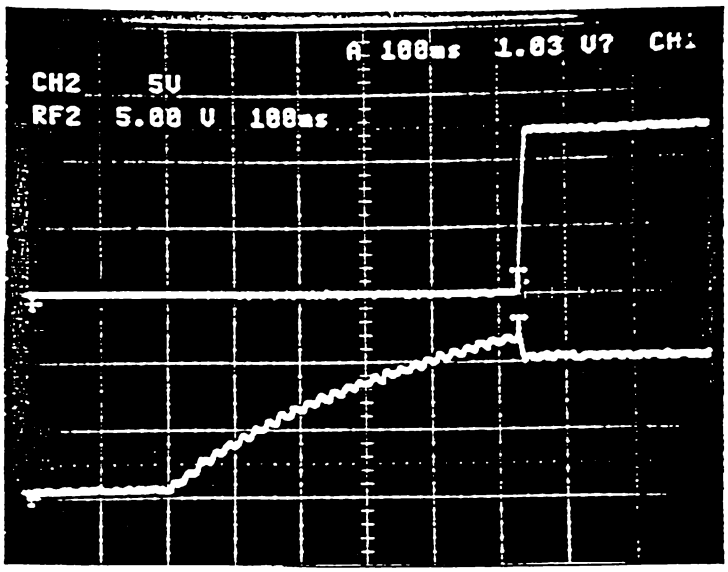
Channel 2: I_{DS}; 0,2 A/Div.



Turn-off Phase of the Powertransistor

Channel 1: V_{DS}; 100 V/Div.

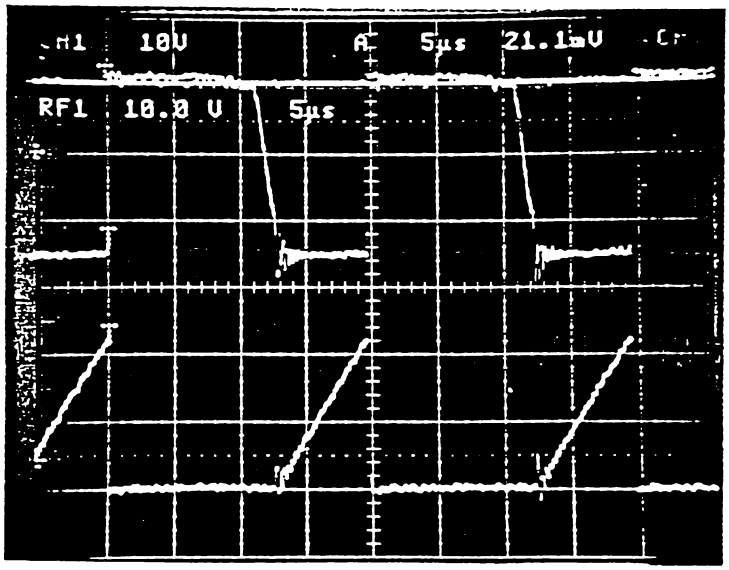
Channel 2: I_{DS}; 0,5 A/Div.



Turn-on of the power supply

Channel 1: Control Voltage

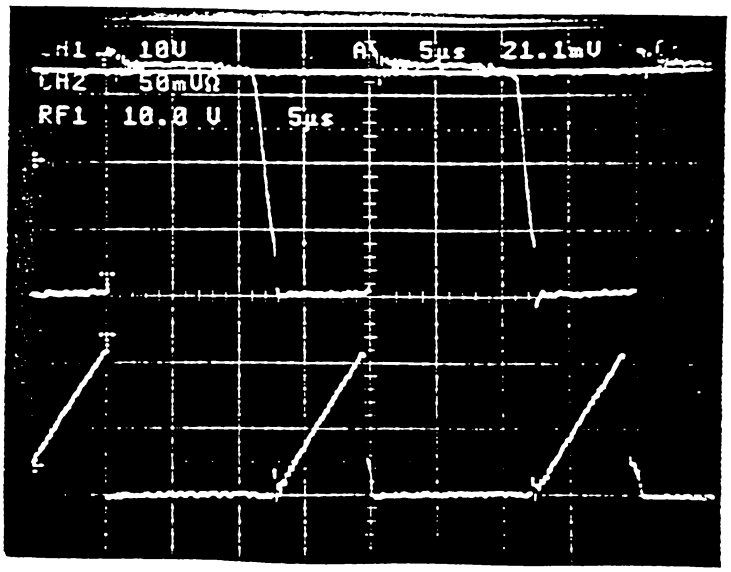
Voltage at C_{110}: 5V/Div.



Supply voltage generation

The upper trace shows the voltage at pin 15 of the transformer during normal operation and the DC level at pin 6 of the integrated circuit with 5 Volt/Div.

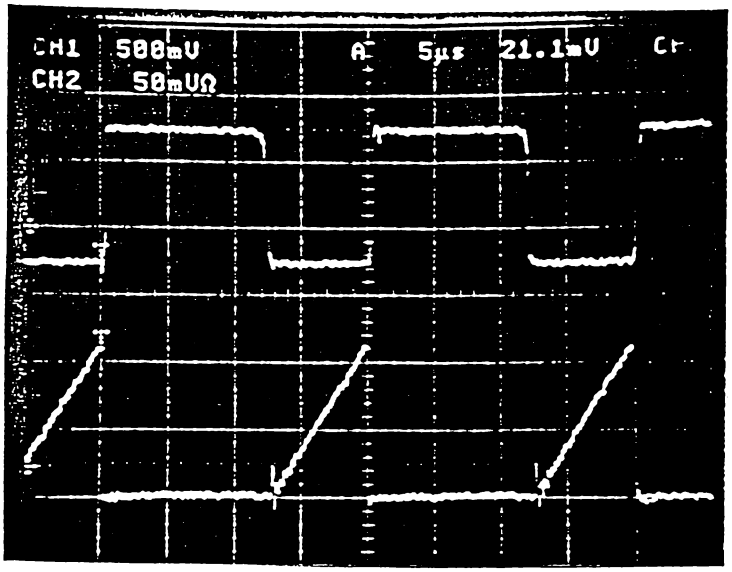
Lower trace: Drain current as reference



Control voltage generation (Voltage at C_{110})

The picture shows the voltage at pin 11 of the transformer and at the load capacitor C_{110} with a resolution of 10V/Div. At pin 1 this DC is divided to approx 400 mV.

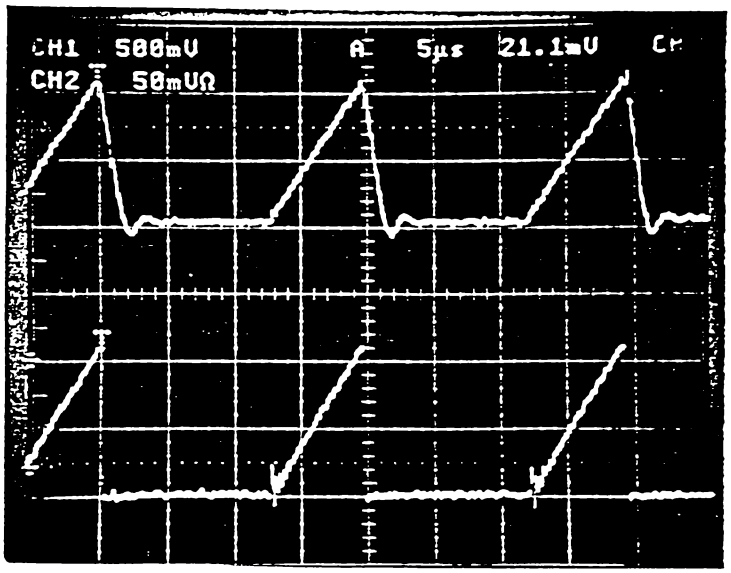
Lower trace: Drain current as reference



The zero crossing at pin 8 of the integrated circuit

Every zero crossing from positive to negative level at pin 8 starts a drain current pulse

Lower trace: Drain current as reference

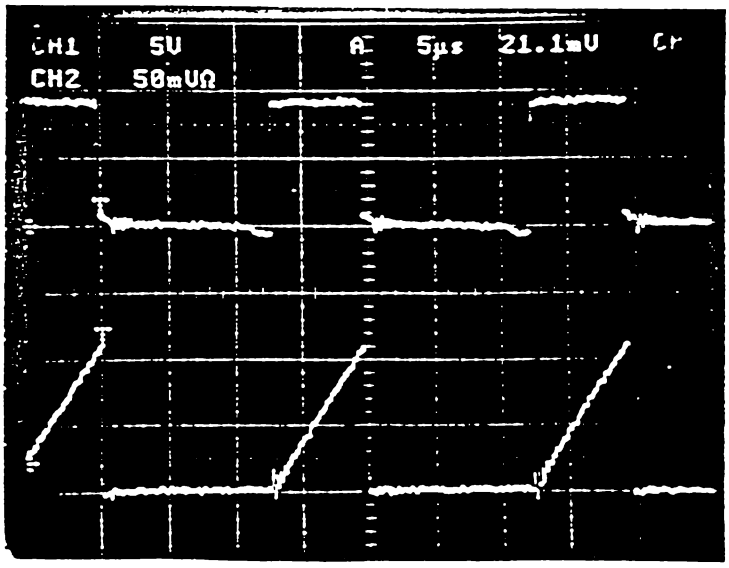


The ramping-up of the drain current simulation voltage at pin 2 of the integrated circuit

The amplitude of this sawtooth is related to the internal error voltage. If the amplitude reaches the error voltage the output pulse is terminated.

Resolution: 0,5V/Div.

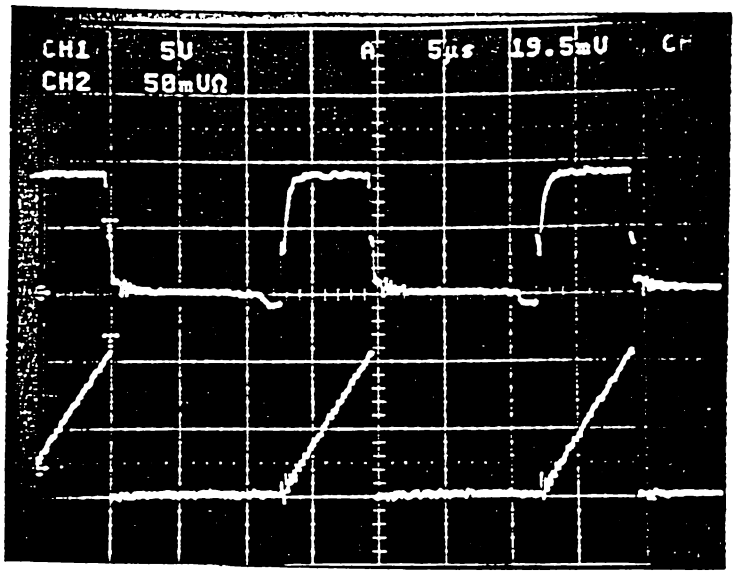
Lower trace: Drain current as reference



Output pulse of the integrated circuit

Voltage at pin 5 of the integrated circuit measured with 5 V/Div.

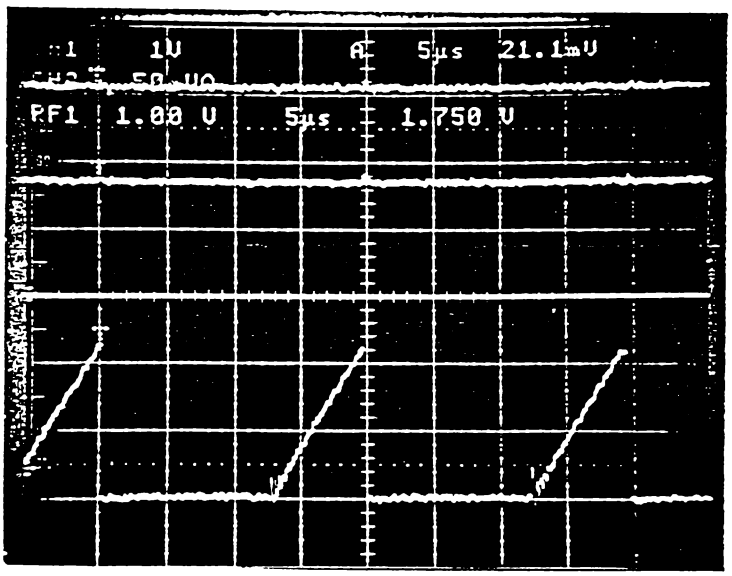
Lower trace: Drain current as reference



Voltage at the gate of the powertransistor

The switching delays related to the Miller effect of the power transistor can be seen at a gate voltage of approx. 4V. The network at the gate increases the switching times of the transistor. Therefore the harmonics of the drain current are reduced.

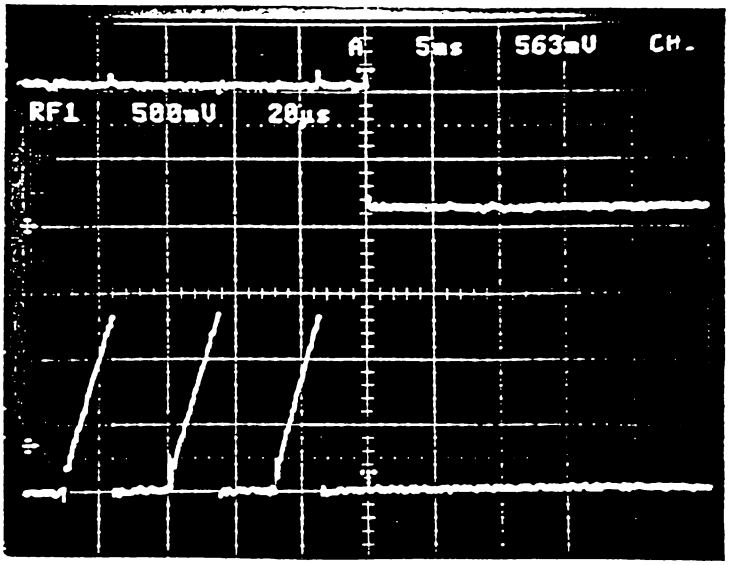
Lower trace: Drain current as reference



DC level at pin 3 and pin 7 of the integrated circuit

At the softstart pin there is a voltage of approx. 3V. At pin 3 there is a level of approx. 1.75V, derived from the primary voltage by means of resistors.

Lower trace: Drain current as reference



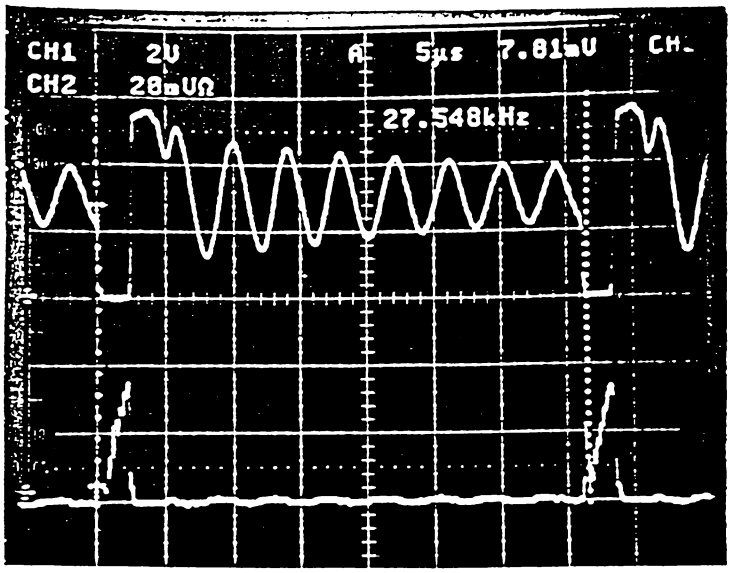
Turn-off due to undervoltage

Channel 1: voltage at pin 3 of the integrated circuit with 0.5 V/Div.

Channel 2: drain current with 1 A/Div.

After the switching level at pin 3 (approx. 1V) is reached, the integrated circuit is clamping the voltage at pin 3 to ground.

Lower trace: Drain current as reference

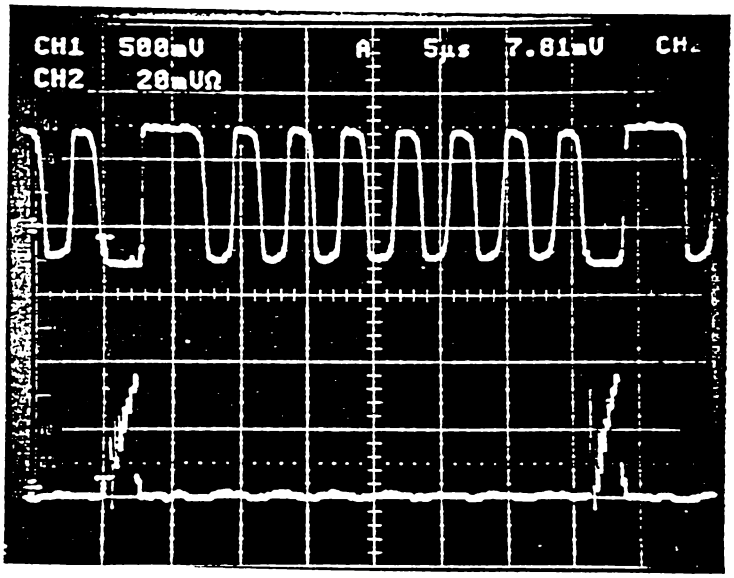


Drainvoltage in Stand-by (4W secondary)

Channel 1: drain voltage with 200 V/Div.

Channel 2: drain current with 1 A/Div.

The integrated circuit reduces the drain current frequenz down to approx. 28 kHz.

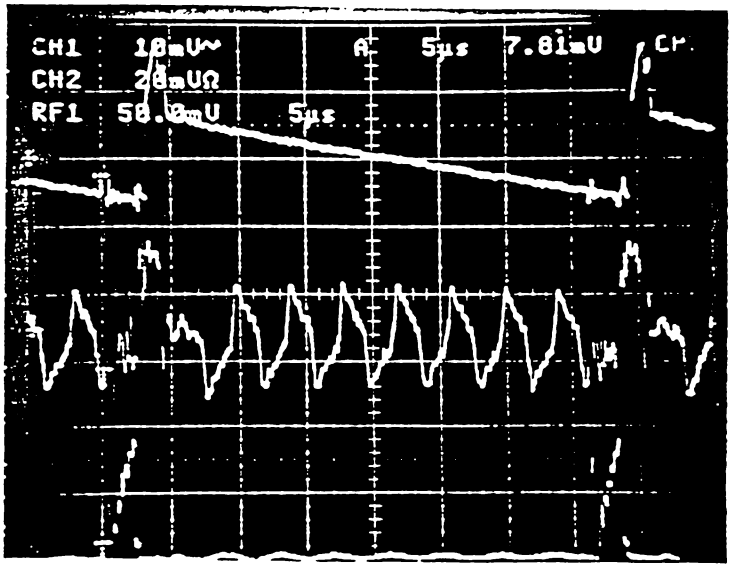


Zero crossing in Stand-by (4W secondary)

Channel 1: Zero crossing signal at pin 8 of the integrated circuit 0.5 V/Div.

Channel 2: drain current as a reference

By suppression of some zero crossings the low frequency is reached.



Function of the Stand-by operation

Channel 1: Voltage at C_{110}; 50mV/Div. AC

Channel 2: differential of the zero crossings by means of R_{115}/C_{109} at pin 1; with 10mV/Div.

They indicate to the PWM a control voltage which is too low, therefore the following drain current pulse is relative big (0,4 A/Div). Therefore the control amplifier is saturated during the following discharge of the transformer. After this voltage is decreased the next pulse is started.